NOX

SUPPLEMENT TO

INTERIM RESEARCH REPORT NO. 11A

PROJECT

lightning

HIGH-SPEED DATA PROCESSOR SYSTEM RESEARCH

Prepared for DEPARTMENT OF THE NAVY
Bureau of Ships, Washington 25, D.C.

Prepared by RADIO CORPORATION OF AMERICA
Camden, New Jersey

Copy No. 116

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Project LIGHTNING

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DEPARTMENT OF THE NAVY

Bureau of Ships, Electronics Division
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Engineering Department
Electronic Data Processing Division
Industrial Electronic Products
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Camden, New Jersey

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TABLE OF CONTENTS

Chapter 1. GENERAL

Chapter 1. GENERAL

1-1 INTRODUCTION

This supplemental report presents material not covered in the main cover of IRR-11A. The main topics are:

- Tunneling Device Research
- Task II
- Task III
- Certain additions in the areas of logic circuits and fabrication techniques

1-2 SUMMARY

A. TUNNELING DEVICES

Tunneling devices governed by the determined electrical specifications have been in production for one month. Development of a supply of crystal which can meet the extremely rigid specifications of the OR diode is a paramount problem. To solve this, an extensive program is underway to grow and evaluate crystal in the required sensitivity range.

The Semiconductor and Material's Division made initial deliveries of tunneling devices for use in Task III circuit development. Included were tunnel diodes with I_p/C ratios of 10 to 1.

Tunnel diodes with I_p/C ratios greater than 10 to 1 were fabricated using the solution alloying/SiO masking techniques. However, these units had low I_p/I_v ratios and high series resistance due to poor "wetting" of electrical contacts. Also, a high-temperature alloying problem is causing difficulty in the fabrication of low-capacitance tunnel rectifiers by this process.

All tunneling devices are being supplied to the Circuits Group in the "two-legged" package using the beam-type screen connector. Future devices will be mounted using thicker Kovar when the required quantity is available. Solution of the solderability problems has resulted in tunneling devices currently being soldered into circuits without major difficulties.

Precision life testing has begun and highly accurate equipment for production testing of tunneling devices is being built. A figure of merit for operating GaAs tunnel diodes without degradation has been established.

B. LOGIC CIRCUIT DEVELOPMENT

The magnetically coupled flip-flop, previously reported on, was improved. Circuit changes resulted in lower recovery time, and improved level sensitivity and loading capability. A problem of resetting this circuit was encountered and a possible solution uncovered.

C. FABRICATION

A tool for bending the cables and studying bending properties of various types of cables was constructed. Also, a wafer holder for the test vehicle was designed and several useful tools to aid in wafer assembly were built. Advanced development designs were proposed for wafers and frames.

D. TASK III - HIGH-SPEED SUBSYSTEM

In order to meet the goals of Task III it has been decided that single-stage tunnel diode gates will be required. Furthermore, these gates will have to be constructed in miniature three-dimensional packages and in such a manner that they may be individually adjusted to tight tolerances.

The work during the first quarter has been very encouraging since several single-stage gates were constructed in miniature packages and experimentally operated at speeds very close to the Task III goals. These experimental results, coupled with the fact that fabrication and measurement techniques are well in hand, make the probability high of meeting the Task III goals within the contract period, provided the necessary tunneling devices are available in adequate quantities. Exact specifications for these devices have not yet been established but will be early in the next quarter. The tolerance and speed requirements will be somewhat stricter than those for Task II-A but the quantities required will be much smaller.

If diodes are available, it is planned to construct a counter to operate at or near the Task III goal speed during the next quarter.

E. TASK IV - INTEGRATED TUNNEL DIODE MEMORY SUBSYSTEM

A .030-inch x .030-inch x .060-inch ceramic package for one memory cell is now being developed. The package will contain one tunnel diode, one tunnel rectifier, and one resistor, and will be suitable for use in strip transmission line applications. Using this package, it is planned to fabricate a prototype memory cell by next quarter. The problem of individually etching the diode and rectifier in this package has been solved by the use of a protective coating of apiezon wax applied in a trichlorethelyne solution.

Chapter 2. COMPUTING DEVICES

SUMMARY

The electrical specifications for all devices required for the logic subsystem have been determined. These devices have been in production for one month. The types of devices required, line yield, and quantity of units shipped during August are as follows:

	Device	Line Yield	Quantity Shipped
(1)	Tunnel Diodes		
	50 ma	11.3%	90
	35 ma		40
	25 ma		68
	20 ma		60
(2)	Clamping Diode	50%	300
(3)	AND Diode	15.4%	225
(4)	OR Diode	5.8%	201

The most urgent problem is to develop a supply of crystal which can meet the extremely rigid voltage and capacitance specifications of the OR diode. Toward this end, an extensive program has been set up to grow and evaluate crystal in the required resistivity range.

Initial deliveries of tunnel diodes and tunnel rectifiers were made to the Laboratories Division for use in the High-Speed Subsystem development. Included in these deliveries were tunnel diodes with an I_p/C of 10 to 1.

Tunnel diodes with an $I_p/C \geq 10:1$ have been fabricated using the solution alloying SiO masking technique. Poor "wetting" of the electrical contact due to the SiO mask has resulted in low peak-to-valley current ratios and high series resistance values for these units. A high-temperature alloying problem is causing some difficulty in the fabrication of low-capacitance tunnel rectifiers by this process.

All tunnel diodes and tunnel rectifiers are being supplied to the Circuits Group in the "two-legged" package using the beam-type screen connector. The Kovar thickness is being changed from .002 inch to .005 inch, and all units will be mounted in packages with the thicker Kovar as soon as the required quantities are available. The solderability problems encountered during the last quarter have been solved, and tunnel diodes and rectifiers are currently being soldered into circuits without any major difficulties.

An investigation of various types of insulating materials, with lower dielectric constants than the ceramic presently being used, has been initiated.

Precision life testing has begun and equipment for measuring production quantities with a high degree of accuracy is being built.

Approximately 365 GaAs tunnel diodes and tunnel rectifiers were either supplied to the Circuits Groups or put on life tests during this quarter.

A figure of merit for operating GaAs tunnel diodes under d-c forward bias conditions, with no degradation, has been empirically established. The requirement to be satisfied is $I_{DC}/C < 0.8$; where I_{DC} is the forward d-c current past the valley, and C is the junction capacitance.

Chapter 2. COMPUTING DEVICES

I. PERSONNEL

The following personnel contributed to this phase of the project during the eleventh quarter:

M. A. Blumenfeld
E. S. Buckley
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E. T. Casterline
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L. J. Vieland
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II. DISCUSSION

A. GERMANIUM TUNNEL DIODES

1. Germanium Tunnel Diode Deliveries

The electrical specifications for the tunnel diodes and tunnel rectifiers were established during this last quarter. The specifications for the four types of tunnel diodes required are tabulated in Table 2-1. All four types are being fabricated by the direct alloying process. In this process, an arsenic-containing dot is alloyed onto a heavily gallium-doped germanium pellet to form the tunneling junction. Typical electrical characteristics of these diodes are tabulated in Tables 2-2 through 2-5.

The rigid specifications regarding current, voltage, and capacitance necessitate strict monitoring of crystal and fabrication processes. With this careful monitoring of these processes, the composite yield is approximately 11%. The units are packaged in five-mil Kovar packages with a screen connector which eliminates parameter changes due to pressure sensitivity.

During the month of August (when the electrical specifications for these diodes were established), the following number of tunnel diodes were shipped to the Circuits Group in Pennsauken:

Type of Diode	Quantity
50 ma	90
35 ma	40
25 ma	68
20 ma	60

TABLE 2-1
ELECTRICAL SPECIFICATIONS FOR 50-, 35-, 25-, AND 20-ma TUNNEL DIODES

Device	I_p (ma)	I_p/I_v	E_p (mv)	E_v (mv)	E_f (mv)	Cap (pf)	R_s (ohms)
50 ma	50 ± 1% (3 groups)	10/1 (min)	99 ± 5%	390 ± 5%	552 ± 2%	12 (max)	1.0 (max)
35 ma	35 ± 1% (3 groups)	10/1 (min)	99 ± 5%	390 ± 5%	552 ± 2%	8.5 (max)	1.3 (max)
25 ma	25 ± 1% (3 groups)	10/1 (min)	96 ± 5%	390 ± 5%	555 ± 5%	6 (max)	1.6 (max)
20 ma	20 ± 1% (3 groups)	10/1 (min)	98 ± 5%	390 ± 5%	555 ± 5%	5 (max)	2.0 (max)

TABLE 2-2
TYPICAL ELECTRICAL CHARACTERISTICS OF 50-ma TUNNEL DIODES

		I_p (ma)	I_p/I_v	E_p (mv)	E_v (mv)	E_F (mv)	R_s (ohms)	Cap (pf)
Electrical Specifications		50 ± 1% (3 groups)	10/1 (min)	99 ±5%	390 ±5%	552 ±2%	1.0 (max.)	12 (max.)
Typical Units	1	50	10.8/1	96	395	555	.7	9.0
	2	49.5	11.2/1	96	400	560	.7	8.5
	3	50	11.9/1	98	400	555	.8	12.0
	4	50	11.9/1	97	400	560	.8	10.0
	5	49.5	12/1	95	400	560	.7	10.5
	6	50	10.8/1	102	390	550	.8	10.2
	7	50	11.6/1	101	395	560	.8	10.0
	8	50	12.2/1	95	400	550	.7	12.0
	9	49.5	11/1	94	390	550	.7	9.6
	10	49	11.1/1	100	400	565	.8	9.0
	11	48.5	12.1/1	98	400	565	.8	10.0
	12	49	10.9/1	104	395	565	.9	8.0
	13	49	10.4/1	103	390	545	.8	11.0
	14	49	13.1/1	94	405	550	.7	10.9
	15	49	12.1	96	395	550	.7	10.0

TABLE 2-3
TYPICAL ELECTRICAL CHARACTERISTICS OF 35-ma TUNNEL DIODES

	I_p (ma)	I_p/I_v	E_p (mv)	E_v (mv)	E_F (mv)	R_s (ohms)	Cap (pf)
Electrical Specifications	35 ± 1% (3 groups)	10/1 (min)	99 ±5%	390 ±5%	552 ±2%	1.3 (max.)	8.5 (max.)
Typical Units 1	35.0	11/1	97	395	555	0.9	8.2
2	34.8	11.6/1	102	395	560	1.2	7.3
3	35.5	11/1	98	395	550	1.1	8.4
4	35.0	11.2/1	100	390	555	1.2	7.5
5	35.0	10.6/1	99	385	545	1.1	7.4
6	35.7	11.9/1	101	395	555	1.1	7.8
7	34.2	11.4/1	99	395	555	1.1	7.4
8	35.0	12/1	100	380	545	1.2	6.8
9	34.5	11.1/1	97	385	545	1.1	7.3
10	35.2	11.3/1	100	395	555	1.1	7.3
11	35.0	10.9/1	96	380	545	1.0	7.5
12	35.0	11.6/1	99	390	550	1.1	7.7
13	35.6	10.4/1	100	385	545	1.1	6.1
14	35.0	10.6/1	104	395	560	1.3	8.5
15	35.2	11.7/1	102	385	560	1.2	7.8

TABLE 2-4
TYPICAL ELECTRICAL CHARACTERISTICS OF 25-ma TUNNEL DIODES

		I_p (ma)	I_p/I_v	E_p (mv)	E_v (mv)	E_F (mv)	R_s (ohms)	Cap (pf)
Electrical Specifications		25 ± 1% (3 groups)	10/1 (min)	96 ±5%	390 ±5%	555 ±5%	1.6 (max.)	6 (max.)
Typical Units	1	24.5	11.9/1	98	395	565	1.4	3.0
	2	24.5	11.1/1	96	395	560	1.3	5.0
	3	24.3	13.4/1	95	400	550	1.4	4.0
	4	24.5	10.9/1	96	395	555	1.2	4.0
	5	25	11/1	97	395	555	1.2	4.6
	6	25	11.6/1	94	405	555	1.3	5.0
	7	25	11.3/1	96	395	555	1.4	5.0
	8	25.5	10.4/1	97	390	555	1.3	5.0
	9	25.2	11.7/1	91	395	545	1.2	6.0
	10	25	12.8/1	95	400	560	1.4	5.5
	11	25.5	11.0/1	97	395	555	1.4	5.0
	12	25	12.1/1	97	400	555	1.4	5.0
	13	25.5	12.7/1	93	395	555	1.3	6.0
	14	25	11.3/1	98	390	550	1.4	5.5
	15	24.8	10.6/1	91	385	540	1.1	5.2

TABLE 2-5
TYPICAL ELECTRICAL CHARACTERISTICS OF 20-ma TUNNEL DIODES

		I_p (ma)	I_p/I_v	E_p (mv)	E_v (mv)	E_F (mv)	R_s (ohms)	Cap (pf)
Electrical Specifications		20 ± 1% (3 groups)	10/1 (min)	98 ±5%	390 ±5%	555 ±5%	2.0 (max.)	5.0 (max.)
Typical Units	1	20.0	12/1	93	400	560	1.4	4.2
	2	19.7	12/1	96	390	550	1.6	4.7
	3	20.0	11/1	95	395	560	1.6	4.8
	4	20.0	11/1	93	400	555	1.5	4.5
	5	19.8	11/1	99	395	560	1.9	4.1
	6	20.0	12/1	95	405	565	1.4	4.3
	7	20.0	12/1	102	405	575	1.9	4.2
	8	20.2	10/1	99	395	565	1.5	4.3
	9	20.0	12/1	99	410	570	1.7	4.5
	10	20.2	10/1	100	395	565	1.7	4.5
	11	20.1	10/1	97	385	545	1.4	4.7
	12	19.4	11/1	95	400	565	1.5	4.5
	13	20.6	11/1	102	405	580	2.0	4.2
	14	19.8	10/1	101	385	565	1.9	4.2
	15	19.4	10/1	97	370	540	1.8	3.8

2. Series Resistance Studies

A study has been made of factors affecting series resistance in the tunnel diode. Figure 2-1 shows an idealized graph of R_S vs junction area. It can be seen that, as junction area becomes very small, series resistance begins to increase rapidly. With the high-speed units presently being fabricated, junction areas are extremely small and operation is in the exponential portion of the curve. Since R_S contributes directly to the peak and forward voltages, which have very tight tolerances, this resistance must be kept as low and as constant as possible.

In examining the series resistance of a tunnel diode, it has been found that contact resistance and package resistance contribute less than .03 ohm and can be considered negligible. Resistance through the alloy dot and semiconductor material varies, however, and can become relatively large.

Before etching, the alloyed pellet appears as shown in Figure 2-2a. The resistance through the unit is a "spreading resistance" and can be approximately calculated by the formula $R_S \cong \rho/2\pi r_o$. For the 25-ma tunnel diode, which utilizes a .004 inch diameter alloy dot and a pellet with a resistivity of approximately 7.8×10^{-4}, this spreading resistance is calculated to be .05 ohm, which is in agreement with laboratory measurements. After etching, the unit exhibits the structure shown in Figure 2-2b. At this stage of the processing the resistance lies mainly in the stem and follows, roughly, the formula for resistance of a cylinder, $R = \rho \ell / A$.

Since the maximum capacitance, and therefore the area, is fixed for the various types of tunnel diodes, the only other variables affecting series resistance are crystal resistivity and length of the stem. The etch structure depends mainly upon two factors: (1) the size of the alloy dot, and (2) the resistivity of the pellet.

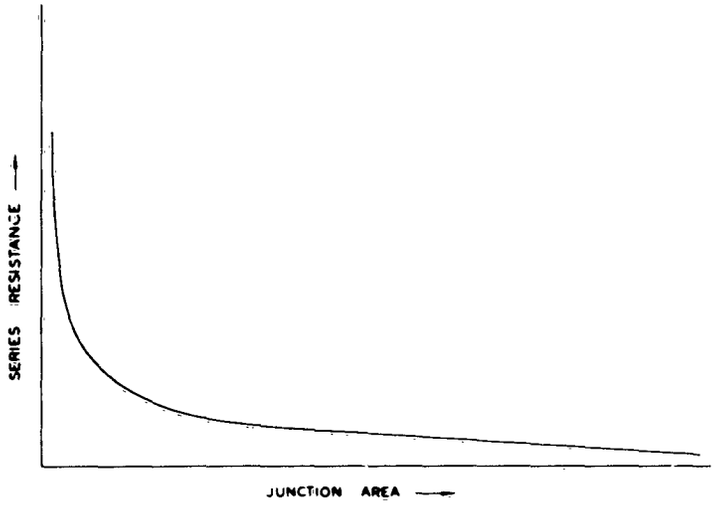


Figure 2-1. Idealized Graph of Series Resistance vs. Junction Area (1)

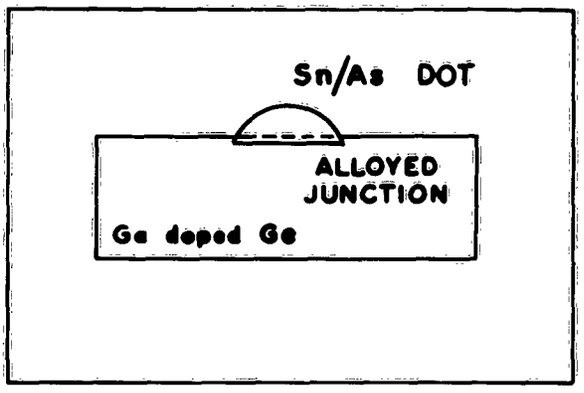


Figure 2-2a. Direct Alloyed Tunnel Diode Before Electrolytic Etching (1)

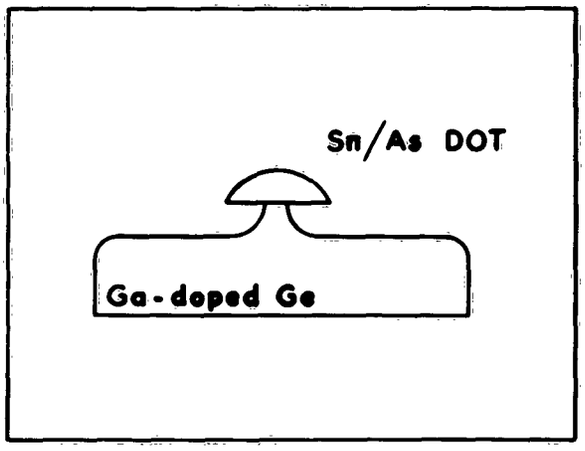


Figure 2-2b. Direct Alloyed Tunnel Diode After Electrolytic Etching (1)

a. Effects of Alloy Dot Size

The size of the alloy dot, used in forming the junction, is the most obvious factor affecting the final etch structure. Since a large alloy dot will form a large initial junction area, a great deal of etching will be required to reduce the area to the desired final diameter of less than .001 inch. In addition, the large dot tends to mask the electrolytic etching action at the junction. As a result, the amount of pellet etched away, and hence the length of the stem, increases markedly as the size of the alloy dot is increased. This is illustrated by the photographs in Figure 2-3. Alloy dots of various sizes were alloyed directly into pellets with a carrier concentration of 1.3×10^{19}. These alloyed junctions were then etched to equal areas (approximately .0007 inch diameter) by monitoring capacitances. Values of series resistance and capacitance are given for each figure, and the increase in R_S due to etch structure is clearly illustrated.

(a) 2-MIL ALLOY DOT
R_s = 1.9Ω
CAP = 3.6pf

(b) 5-MIL ALLOY DOT
R_s = 2.2Ω
CAP = 3.4pf

(c) 7.5-MIL ALLOY DOT
R_s = 4.3Ω
C = 3.4pf

(d) 11-MIL ALLOY DOT
R_s = 8.6Ω
C = 3.4pf

Figure 2-3. Alloyed Dots of Various Sizes (1)

Figure 2-4 shows a curve of R_S vs. alloy dot size for pellet impurity concentrations of 1.3×10^{19} and 6.1×10^{19}. The increase of series resistance with dot size can be seen in both curves. This increase, however, is much more drastic for the lower carrier concentration material.

b. Effects of Crystal Resistivity

Series resistance is also dependent upon the resistivity of the pellet, both for the unetched diode ($R_S \cong \rho/2\pi r_o$) and also after etching ($R_S \cong \rho\ell/A$). In Figure 2-5, R_S is plotted against carrier concentration for tunnel diodes before etching and after etching to a .001 inch diameter. The large increase in R_S of the etched units at low carrier concentrations can be shown to be due not only to the resistivity factor (ρ) in the formula $R \cong \rho\ell/A$, but also to an increase in the length of the stem.

It has been observed that high-concentration crystal tends to etch more rapidly and more selectively at the junction than lower doped material. This effect is shown in the photographs in Figure 2-6. In this study, .006 inch diameter Sn/As dots were alloyed onto pellets of various resistivities. These units were then electrolytically etched to equal areas (approximately .0006 inch diameter). The resulting etch structures show the high-concentration crystals to have a shorter stem. This effect is also illustrated in Figure 2-7 where R_S has been plotted against crystal resistivity. If the etch structure were identical in all cases, R_S should be directly proportional to the value of crystal resistivity, and the curve would follow the straight line indicated. However, the rapidly increasing R_S at high values of resistivity indicates that the length of the stem becomes a factor. This change of etch structure with carrier concentration also explains the difference in form of the two curves in Figure 2-4.

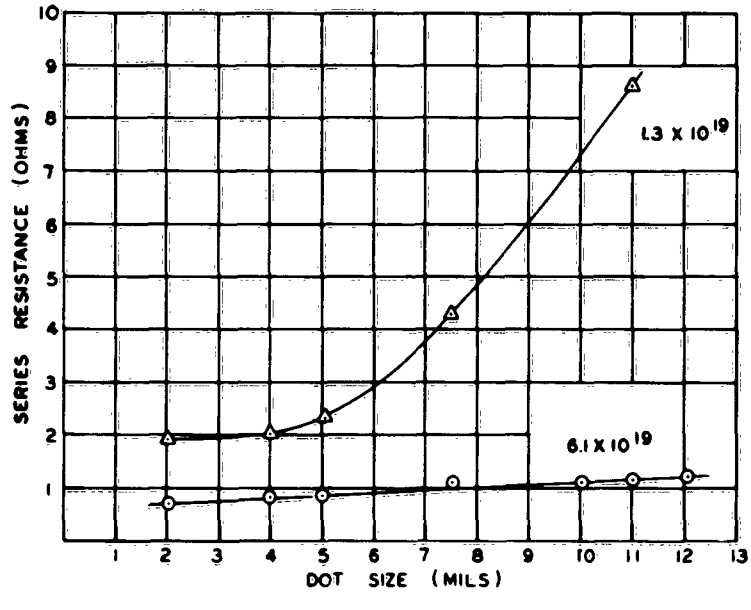


Figure 2-4. Series Resistance vs. Alloy Dot Size (Units Etched to 7-Mil Dia.) (1)

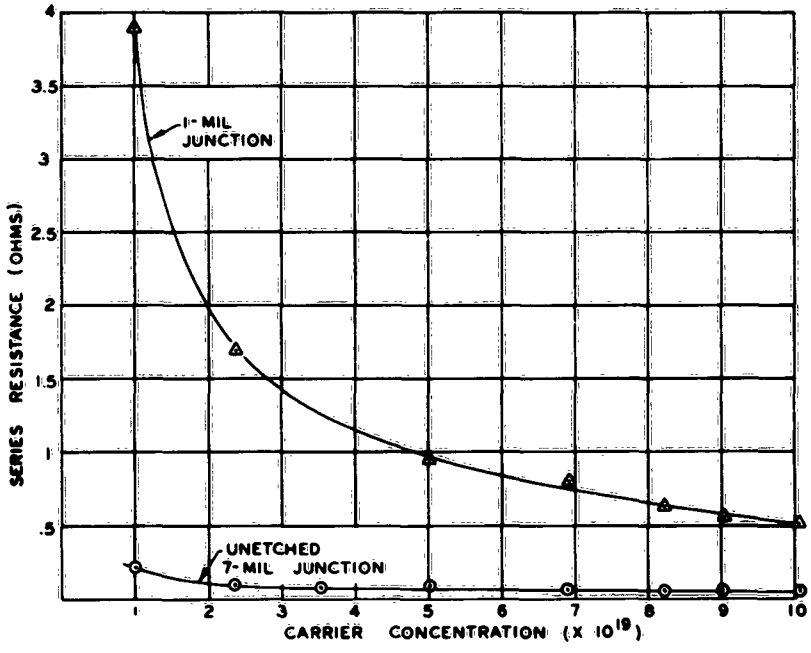


Figure 2-5. Series Resistance vs. Carrier Concentration (4)

These studies show that series resistance can be controlled by the choice of alloy dot size and crystal resistivity, and this knowledge has been incorporated into the design of tunneling devices. The size of the alloy dot used in fabricating tunnel diodes has been reduced from .006 inch to .004 inch as mounting techniques have improved. For the clamping diode, where R_s is very critical, a .003 inch alloy dot is used. This appears to be the lower limit of dot size for production work. In addition, both the clamping diodes and tunnel rectifiers utilize very low-resistivity crystal to minimize R_s. In these cases, since the I_p/I_v ratio is not critical, very high alloying temperatures can be used to reduce the peak currents sufficiently. In addition to minimizing series resistance, a short-stem configuration after etching contributes much to the mechanical stability of the unit.

3. Germanium Clamping Diodes

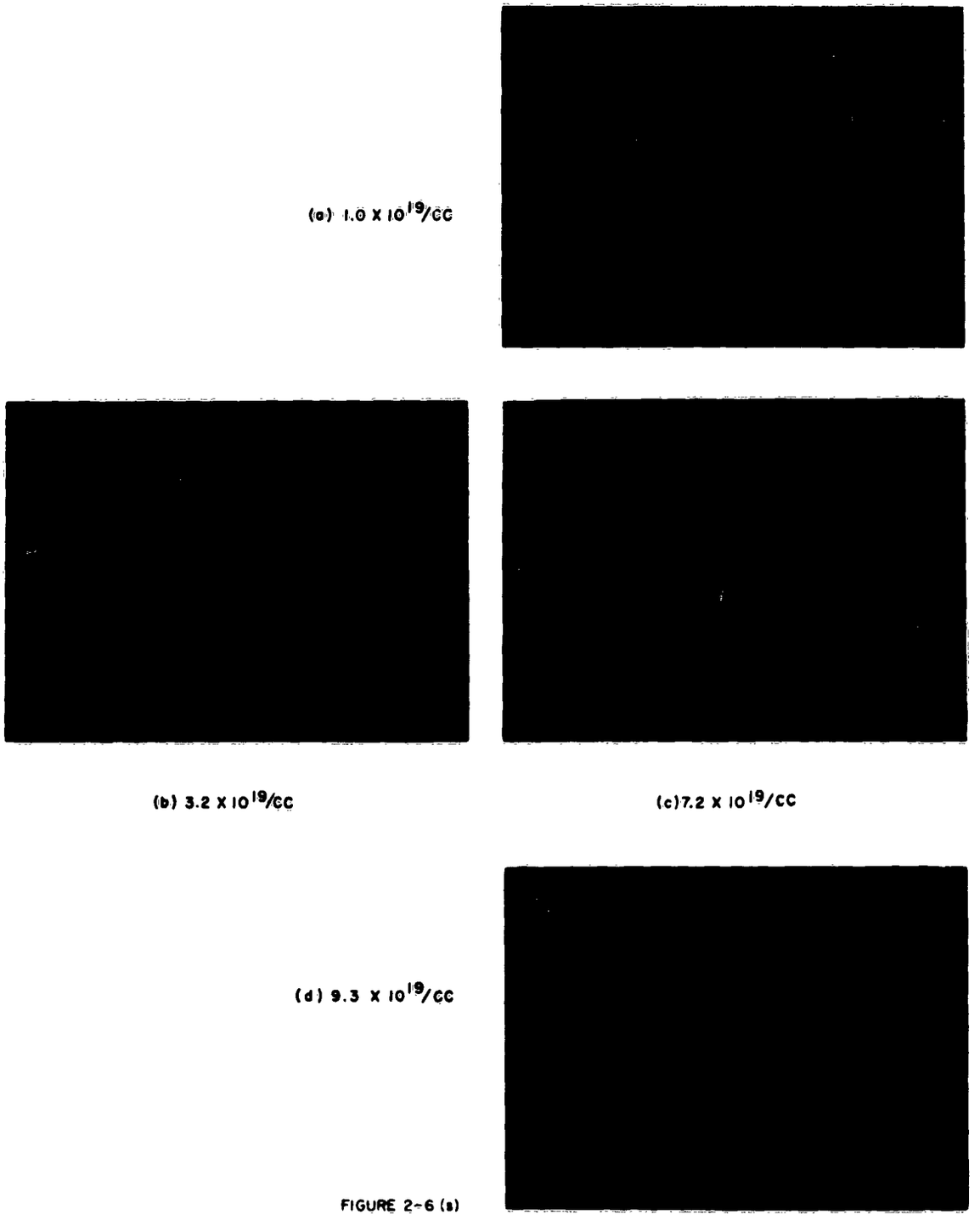
Specifications for the clamping diode have been established as follows:

$I_p \leq 0.7$ ma

Cap = 8 pf max.

E_R at 60 ma (reverse) = 190-220 mv

The clamping diode is fabricated by alloying a 3-mil arsenic-containing dot directly into a gallium-doped germanium pellet (doped to $3.5\text{-}4.0 \times 10^{19}$ atoms/cc). The alloy cycle is 550°C for 2 minutes. To achieve the low series resistance value



(a) 1.0×10^{19}/cc

(b) 3.2×10^{19}/cc

(c) 7.2×10^{19}/cc

(d) 9.3×10^{19}/cc

FIGURE 2-6 (a)

Figure 2-6. Etching and Carrier Concentration (a)

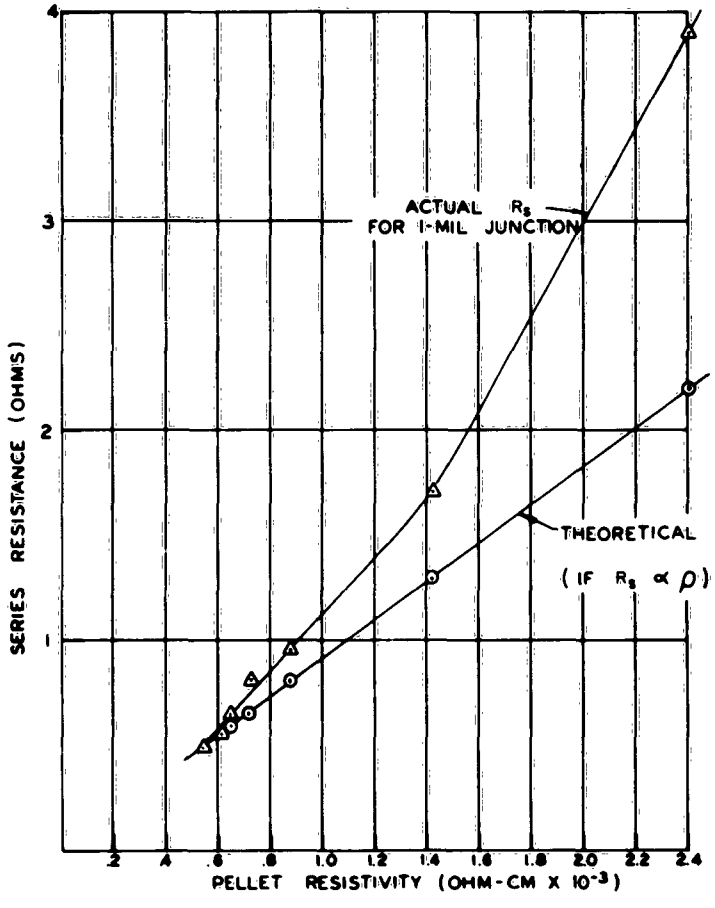


Figure 2-7. Series Resistance vs. Pellet Resistivity [5]

necessary to meet the reverse voltage specification, the size of the alloy dot has been reduced to 3-mils diameter. The impurity concentration in the pellet is fairly high. By using a very high alloying temperature (550°C), the peak currents are reduced to the desired range. These units are packaged in the conventional tunnel diode package using the screen connector.

Typical electrical characteristics of these units are shown in Table 2-6.

During the month of August, 300 clamping diodes were supplied to the Circuits Group at Pennsauken.

TABLE 2-6
TYPICAL ELECTRICAL CHARACTERISTICS OF CLAMPING DIODES

Electrical Specifications	I_p (ma) 0.7 max.	Cap (pf) 8.0 max.	E_R (mv) at 60 ma 205 ±7%
Typical Units			
1	.37	6.8	215
2	.66	5.2	215
3	.54	6.2	215
4	.53	5.0	210
5	.52	5.8	215
6	.59	5.8	215
7	.33	7.9	215
8	.42	5.2	215
9	.54	5.2	215
10	.65	4.7	220
11	.62	5.1	220
12	.41	5.8	220
13	.63	6.1	215
14	.42	8.0	210
15	.69	5.2	220

4. Germanium Tunnel Rectifiers

The electrical specifications established for the AND and OR germanium tunnel rectifiers are as follows:

	I_p (ma)	E_F (mv)	Cap (pf)	E_R (mv)
AND Diode	≤ 0.5	-	≤ 3.0	134±5%
OR Diode	≤ 0.2	480-520 at 1 ma	≤ 1.0*	162±5%

*3 out of every 19 diodes may have capacitances ≤ 1.2 pf.

The AND diode is presently being fabricated in a 2-mil Kovar package having a 40-mil ceramic spacer. Yields on this type are 15% and, during August, 225 AND diodes have been shipped to the Circuit Group in Pennsauken. Typical electrical characteristics of these units are shown in Table 2-7.

TABLE 2-7
TYPICAL ELECTRICAL CHARACTERISTICS OF AND DIODES

Electrical Specifications	I_p (ma) 0.5 max.	Cap (pf) 3.0 max.	E_R at 10 ma (mv) 134 ± 5%
Typical Units			
1	.47	2.0	132
2	.42	2.3	128
3	.36	2.1	130
4	.31	1.8	134
5	.30	2.9	130
6	.37	2.0	132
7	.33	2.1	128
8	.50	1.8	132
9	.45	2.1	130
10	.44	2.8	130
11	.34	1.8	132
12	.49	2.1	130
13	.42	1.9	128
14	.35	3.0	132
15	.43	1.6	132

The OR diode is much more difficult to fabricate because of the tighter tolerances and the small junction area required. For this unit a 5-mil Kovar package and a 0.2-mil thick, gold-plated screen is being used as a connector tab. Because of the small junction areas (less than 0.3 mil), these units are quite fragile and must be handled with extreme care until they are encapsulated. The yield on this unit was 5.8% for the month of August.

During August, 201 OR diodes were shipped to the Circuits Group in Pennsauken for use in the logic subsystem. Typical electrical characteristics of these units are shown in Table 2-8.

In order to increase the yield and continue supplying OR diodes in the required amounts, a number of difficulties must be overcome.

The most urgent need is to develop a supply of crystal which can meet the extremely rigid voltage and capacitance specifications of the OR diode. Toward this end, an extensive program has been set up to grow and evaluate crystal in the required resistivity range. In addition, a more long-range basic-study program has been established to examine the effect of crystal parameters on the electrical characteristics of tunnel diodes.

TABLE 2-8
TYPICAL ELECTRICAL CHARACTERISTICS OF OR DIODES

Electrical Specifications		I_p (ma) 0.2 max.	Cap (pf) 1.0 max. 1.2 max.	E_R at 7.5 ma (mv) 162 ± 5%	E_F at 1 ma (mv) 480-520
Typical Units	1	.186	1.1	160	495
	2	.136	0.9	160	505
	3	.086	0.9	165	500
	4	.080	0.9	165	500
	5	.088	0.9	165	510
	6	.082	1.0	165	500
	7	.080	1.1	165	500
	8	.076	0.9	165	500
	9	.068	1.0	170	500
	10	.090	0.9	168	485
	11	.068	1.0	162	480
	12	.136	1.0	162	480
	13	.100	1.1	166	480
	14	.120	1.1	166	480
	15	.150	1.1	167	485

Improvements in yield are also possible by reducing the present package capacitance (0.3-0.35 pf) which adds to the capacitance of the unit. This additional capacitance is sufficient to cause a large number of units to be out of specifications. A package with a lower capacitance is now being designed to alleviate this difficulty.

5. Germanium Tunnel Diodes and Tunnel Rectifiers for High-Speed Subsystem

A total of 104 units (Ge and GaAs tunnel diodes and Ge tunnel rectifiers) have been delivered to the Laboratories Division for circuit development work on the High-Speed Subsystem. Several of the tunnel diodes in this group had peak current-to-capacitance ratios of 10 to 1.

In an effort to eliminate package capacitance, the design shown in Figure 2-8 is being evaluated at the Laboratories Division. Initial attempts to supply low-capacitance units (approx. 3 pf) in this package were not successful. The package dimensions required the use of smaller size pellets which had insufficient mass to allow etching of the units to the necessary low-capacitance value. To correct this situation a modification, which will allow the use of larger-size pellets, has been made in the package.

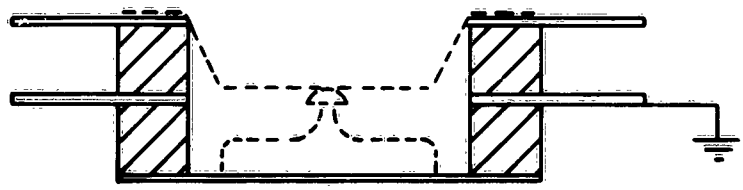


Figure 2-8. Tunnel Diode Package with Ground Ring (a)

6. Silicon Monoxide Masking Technique

a. Tunnel Diodes

High-speed germanium tunnel diodes, with I_p/C ratios of 10 to 1, have been fabricated using the silicon monoxide mask in conjunction with the solution alloying process. There has been some difficulty, however, in obtaining good peak-to-valley current ratios and low series resistance values for these high-speed units. It is believed that these poor electrical characteristics are a result of the inability of the lead contact dot to "wet" or adhere to the surface of the SiO mask. Instead of "wetting" in the SiO, the lead bridges the surface and a device, which is pressure sensitive (low I_p/I_v) and which has poor electrical contact (high R_s), is obtained. To provide a surface which will be "wet" by the lead contact dot, it is planned to evaporate a suitable metal over the SiO mask after the solution alloying process has been completed.

b. Tunnel Rectifiers

The fabrication of tunnel rectifiers requires that high-concentration base wafers be alloyed at high temperatures to obtain low resistivity material and p-n junctions with low peak current densities. The present difficulty being experienced with the fabrication of these units is in forming p-n junctions at a temperature high enough to reduce the peak current density to the desired levels. Results indicate that saturation with germanium of the melt is occurring at a temperature lower than the theoretically calculated value. Therefore, by increasing the percentage of germanium in the melt, it should be possible to achieve higher junction formation temperatures and the desired lower peak current densities should result.

7. Tunnel Diode Package Development

All tunnel diodes and tunnel rectifiers are being supplied to the Circuits Group in the "two-legged" package using the beam-type screen connector. The Kovar thickness is being changed from .002 inch to .005 inch to improve the mechanical stability and

thermal resistivity of the packaged units. The following improvements have been observed using .005 inch Kovar packages:

(1) Units are less pressure sensitive;

(2) Shrinkage from soldering operations is reduced.

Due to the limited supply of .005 inch Kovar packages presently available, only AND and OR diodes are being supplied in this type package. Tunnel diodes and clamping diodes will be mounted in packages made with the thicker Kovar when the required quantities are available.

a. Solderability

The solderability problems encountered during the last quarter have been solved and tunnel diodes and rectifiers are currently being soldered into circuits without any major difficulties. Units are presently being supplied with the "legs" of the package tinned on both sides and bent at an angle of 180° to each other.

Initially the "legs" were tinned on one side only, using a heated iron and 60/40 solder. This did not work satisfactorily however, and it was determined that both sides of the "legs" must be tinned to obtain good solder connections. In order to tin both sides, dip soldering was investigated. The first tests on this method were made using 60/40 solder, but the high temperature required to obtain good "wetting" resulted in changes in the electrical characteristics of the units. A solder (bismuth) having lower melting temperature was investigated next but good "wetting" of the solder to the package could not be obtained. To improve "wetting", a solder consisting of 50% tin - 50% indium and a low-boiling-point activated resin flux was evaluated. This combination of solder and flux gave very good "wetting" at a low temperature, and units did not change in electrical characteristics after being tinned by this process.

b. Screen Mounting

The bar-type screen connector is now being used on all tunnel diodes and tunnel rectifiers. Using this type of connector made it possible to use smaller alloying and contact dots thereby reducing the amount of pellet dissolved during the etching operation. This has resulted in units which are more mechanically stable and which have lower series resistance. The use of a screen has also reduced the amount of tension on the diode junction. This has improved the etching yield and also helped to reduce the pressure sensitivity of the units.

The optimum size of the screen material has not yet been determined and the following three types are currently being evaluated:

Screen Thickness	Lines Per Inch
0.1 - 0.2 mil	500
0.2 - 0.3 mil	333
0.4 - 0.5 mil	250

c. Capacitance

The low capacitance values required for tunnel rectifiers and very high-speed tunnel diodes ($I_p/C \geq 10{:}1$) have necessitated a reduction in the package capacitance. In view of this, the investigation of various types of insulating materials (with lower dielectric constants than the ceramic presently being used for the package insulator) has been initiated. Some of the materials which will be evaluated are: (1) glass, (2) quartz, (3) fosterite, and (4) plastic.

d. New Package

The tooling for the new package with a bridge-type beam connector has been completed. Some minor reworking of this tooling was required. To date, no packages within specification have been received.

8. Germanium Tunnel Diode Life Test Data

Germanium tunnel diode life tests, with parameters being read to better than 1% accuracy, were initiated on a small scale during this quarter. Five-ma and 50-ma units were operated at a forward current of I_p + 10% at 25°C. Results to date are shown in Figures 2-9 and 2-10. Variables that may have affected these results are (1) Pressure (the units had to be individually handled during each measurement); (2) Temperature (changes of ± 1°C were noted between measurement periods); and (3) Quality of units (no attempt was made to assure that all units were initially within specifications).

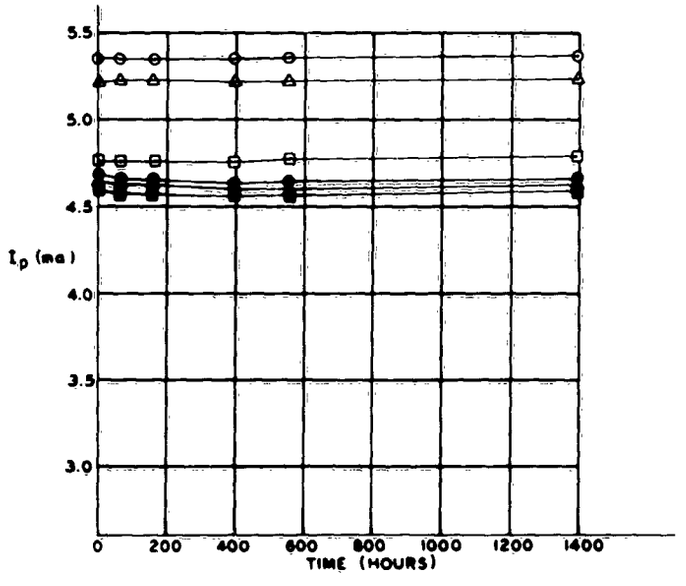


Figure 2-9. I_p vs. Time (5-ma Unit; Operating Conditions — I_p +10% at 25°C) (1)

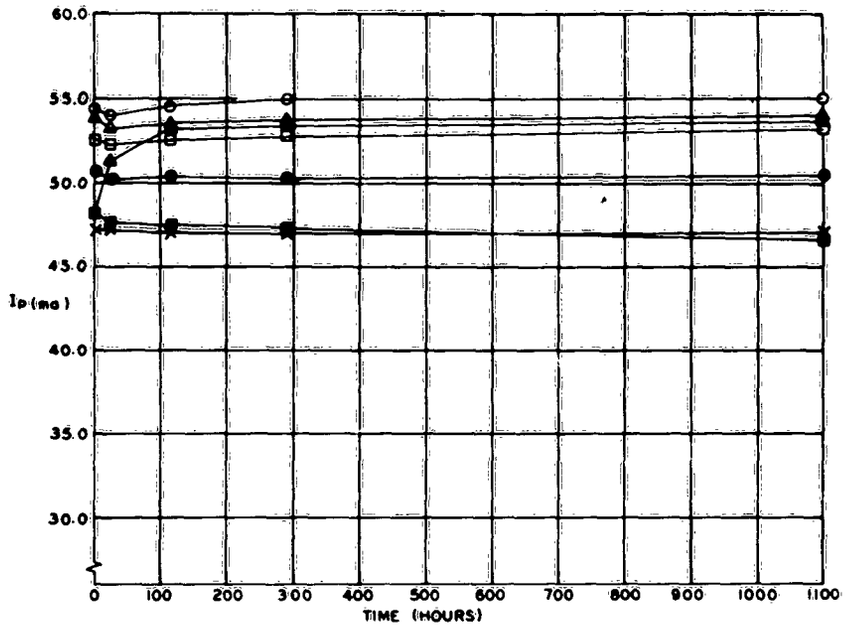


Figure 2-10. I_p vs. Time (50-ma Units; Operating Conditions — I_p +10% at 25°C) (1)

In future precision life tests, the above mentioned variables will be controlled by: (1) mounting units on printed circuit cards; and (2) making measurements in a controlled temperature region.

The large-scale precision life test program will be initiated as soon as the necessary equipment is installed, probably during the next quarter.

Test sets for the tunnel rectifiers have been built and are now being calibrated. These sets will enable the taking of readings on production quantities of rectifiers with an accuracy of better than 1%. The Circuits Group will receive a test set identical to the one used at the Semiconductor Division, thus enabling the former to recheck units when desired.

B. GALLIUM-ARSENIDE TUNNEL DIODES

1. Gallium-Arsenide Tunnel Diodes and Tunnel Rectifiers for the Memory Subsystem

a. Diffusion Process

During this quarter, electrical specifications were established for all GaAs devices required for the memory subsystem. These specifications, which are

shown in Table 2-9, are based on diodes made by the diffusion process. The I_p/C ratio was set at 2 to provide sufficient speed while simultaneously allowing a degree of safety in the operation of the GaAs tunnel diodes.

TABLE 2-9
SPECIFICATIONS FOR MEMORY SUBSYSTEM DEVICES

Device	I_p (ma)	I_p/I_v	E_p (mv)	E_v (mv)	E_F (mv)	R_s (ohms)	Cap (pf)
50 ma	47.5-52.5	10/1 min	140-155 155-170 170-190 (3 groups)	500-580	1020-1180	2.5 (max)	20-30
100 ma	95-105	10/1 min	180-200 200-220 220-240 (3 groups)	530-620	1040-1200	1.5 (max)	40-60
250 ma	240-260	10/1 min	205-225 225-250 250-275 (3 groups)	530-620	1050-1220	1.0 (max)	100-150

The specifications were in effect for devices scheduled for delivery, and highly satisfactory yields were consistently demonstrated.

At present, the diffusion process is being held in abeyance because of the request from the Circuitry Personnel to explore the solution alloying process. GaAs diodes made by the solution alloying process offer the possibility of an increased voltage swing ($\Delta E = E_F - E_p$) which would be highly desirable from the standpoint of the circuitry.

b. Solution Alloying Process

As of August 1, work was started on developing specifications for GaAs tunnel diodes made by the solution alloying process. Thus far, several different epitaxial crystals were processed into 50-ma, 100-ma, and 250-ma tunnel diodes. The resulting product shows the hoped-for gain in voltage swing, and new electrical specifications will soon be proposed on a statistical basis.

For these diodes, the I_p/C ratio constituted a problem parameter because the epitaxial type crystal is usually very highly doped. As such, it inherently yields very

fast (high I_p /C ratio) tunnel diodes if a standard process is employed. However, with the use of a controlled degradation process which results in a broadening of the depletion layer width, the required I_p/C values can be obtained. The unit is subsequently etched to the required peak current value.

The yield with this process is highly satisfactory. Further work will be required to determine how critical is the quality of the solution grown (epitaxial) crystal.

c. P on N GaAs Tunnel Diodes

In order to make tunnel diodes using doping materials other than zinc and tin, some p on n junction diodes were made by alloying cadmium dots to unoriented selenium doped crystal. The resultant tunnel diodes had poor peak-to-valley current ratios (about 3 to 1), but may be useful as tunnel rectifiers. No life tests on these units have been conducted. More work on p on n type diodes is planned, particularly in view of the lower resistivity of n-type crystal for similar carrier concentrations.

d. GaAs Tunnel Rectifiers

Electrical specifications for the GaAs tunnel rectifier have been further tightened and are as follows:

$I_p \leq 0.5$ ma

$E_{R\ (4\ ma)} \leq 215$ mv

$E_{F\ (1\ ma)} = 1050$ mv ± 10%

$C \leq 2.0$ pf

In order to fabricate these low-capacitance units at satisfactory yields, a masking technique is now being used in conjunction with the solution alloying process.

Thus far, the plane which offers the best results for epitaxial growth is the $\bar{1}\bar{0}\bar{0}$ plane. Au-Ge-Sn dots are now being used for the n-type dopant.

Typical electrical characteristics of units being supplied to the Circuits Group are shown in Table 2-10.

e. Deliveries and Life Testing

The following numbers of various units have been delivered to the Circuits Group/Laboratories Division, or put on life test during the reported period.

Type	Shipped	Life	Sub Total
Rectifiers	80	29	109
50-100-250-ma TD's	128	126	254
Sub Total	208	155	Grand Total 363

TABLE 2-10
TYPICAL ELECTRICAL CHARACTERISTICS OF GaAs TUNNEL RECTIFIERS

	I_p (ma)	Cap (pf)	E_R at 4 ma (mv)	E_F at 1 ma (volts)
Electrical Specifications	0.5 (max)	2.0 (max)	215 mv (max)	1.050 ± 10%
Typical Units				
1	.17	1.6	205	1.15
2	.16	2.0	195	1.10
3	.17	1.8	195	1.15
4	.32	1.4	170	1.14
5	.37	1.8	140	1.15
6	.50	2.0	145	1.02
7	.14	1.4	215	1.15
8	.44	1.8	125	1.00
9	.50	2.0	215	1.10
10	.21	1.7	200	1.15
11	.45	1.9	165	1.10
12	.11	1.5	215	0.95
13	.33	1.8	190	1.05
14	.24	1.2	210	1.15
15	.43	2.0	170	1.15

2. Tunnel Diode Degradation Studies

Three aspects of the degradation problem have been studied. These are: (1) a study of the conditions under which diodes may degrade; (2) a study of fabrication techniques directed toward reducing or eliminating the degradation; and (3) a study of the degradation mechanism.

a. Conditions for Degradation

(1) DC Life Tests

Great emphasis has been placed on life testing of GaAs tunnel devices. Tests covering a wide range of types (e.g., rectifiers and 1-ma, 5-ma, 50-ma, 100-ma, and 250-ma diodes) representing various switching speeds (I_p /C) have been conducted under various forward operating (DC) currents. The tests which have been completed are summarized in Figures 2-11 through 2-15 and the details are tabulated in Table 2-11.

TABLE 2-11
SUMMARY OF LIFE TESTS OF GaAs TUNNEL DIODES

Figure No.	Type	Operated	Duration
2-11	1 ma	at 5 ma DC	636 Hours
2-12	5 ma	Consecutive	
		5 ma	140 hours
		10 ma	470 hours
		20 ma	367 hours
2-13	50 ma	Parallel Test	
		10 ma	780 hours
		25 ma	780 hours
		50 ma	301 hours
2-14	100 ma	Parallel Test	
		25 ma	1050 hours
		50 ma	1050 hours
		125 ma	470 hours
2-15	250 ma	Parallel Test	
		50 ma	880 hours
		120 ma	880 hours

All the tabulated tests were carried out on diffused-type units.

The data summarized in Figures 2-11 through 2-15 further emphasize what was noted in previous reports, that the degradation rate of GaAs tunnel diodes depends on both the diode ratio (I_p/C) and the quiescent operating point. Most obvious degradation occurs to the units I_p, E_F, E_v, and E_p, while the changes of I_v, R_s, and capacitance are relatively small.

A figure of merit for operating GaAs tunnel diodes under d-c forward bias conditions, with no degradation, has been empirically established. The requirement to be satisfied is: $I_{DC}/C \leq 0.8$, where I_{DC} is the forward d-c current past the valley, and C is the junction capacitance measured at the valley. This figure of merit applies to diodes with high peak currents which are operated at less than I_p in the forward direction. It also applies to low-current units operated at currents greater than I_p. Figure 2-16 shows typical degradation curves (relative change in I_p vs. diode speed ratio I_p/C) for 100-ma units operated at 25-ma past the valley and 1-ma units operated at 5-ma forward current. In both cases, diodes for which $I_{DC}/C < 0.8$ showed essentially no degradation, whereas diodes for which this value was exceeded did show degradation.

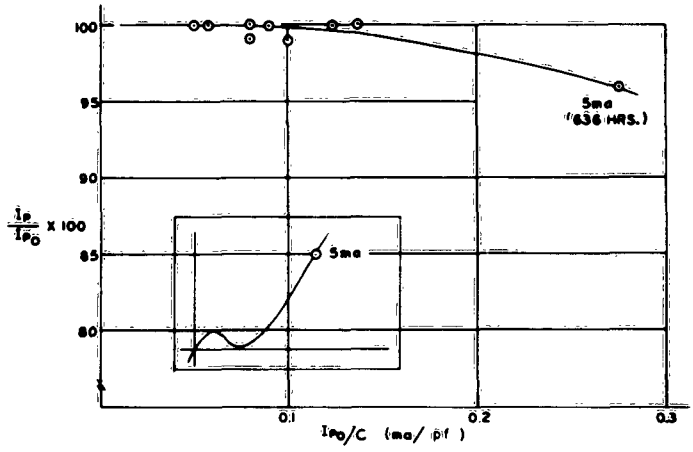


Figure 2-11. Life Data of 1-ma GaAs Tunnel Diode (Diffused) Tested at 5-ma Operating (D C) Current for 636 Hrs. (s)

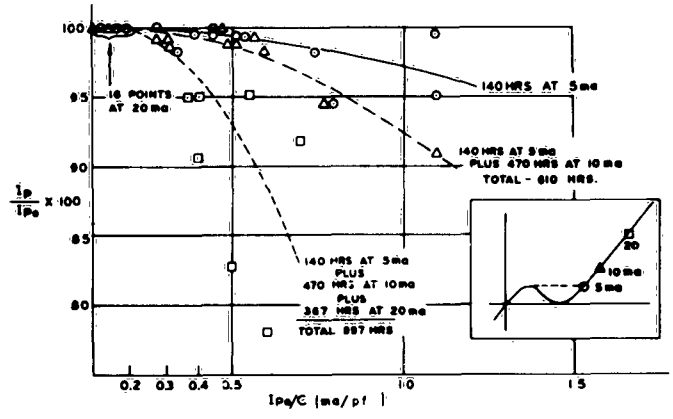


Figure 2-12. Life Data of 5-ma GaAs Tunnel Diodes (Diffused) Tested at Various Operating (D C) Currents Beyond the Valley (s)

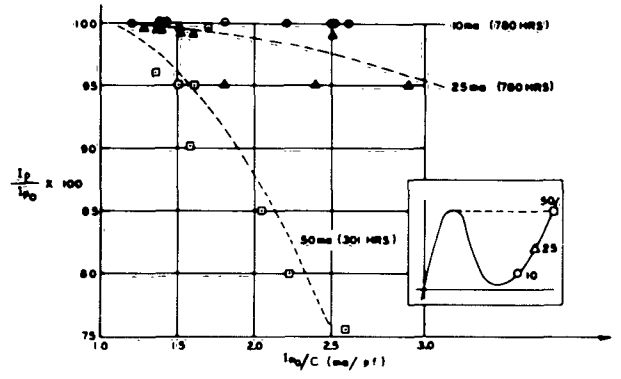


Figure 2-13. Life Data of 50-ma GaAs Tunnel Diodes (Diffused) Tested at Various Operating (D C) Currents Beyond the Valley (s)

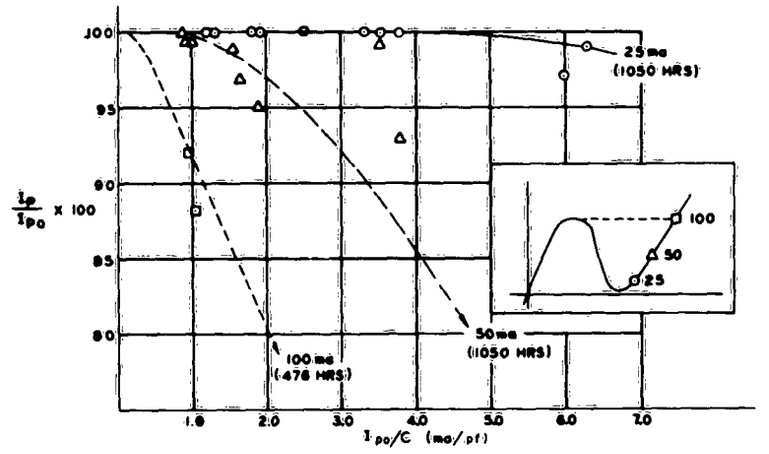


Figure 2-14. Life Data of 100-ma GaAs Tunnel Diodes (Diffused) Tested at Various Operating (D C) Currents Beyond the Valley (s)

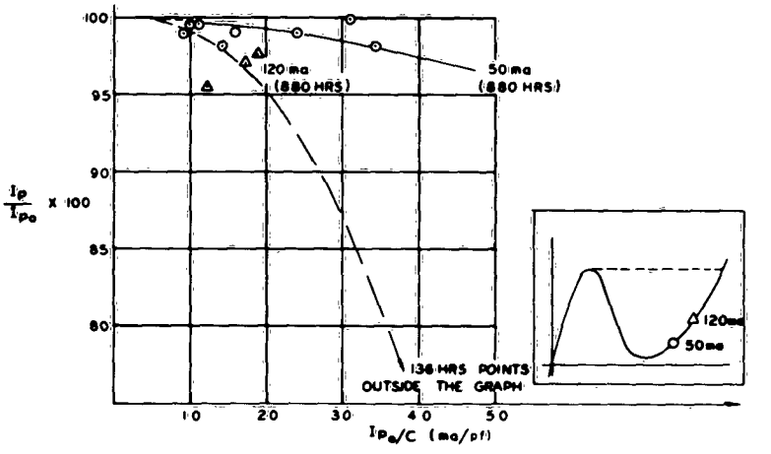


Figure 2-15. Life Data of 250-ma GaAs Tunnel Diodes (Diffused) Tested at Various Operating (D C) Currents Beyond the Valley (s)

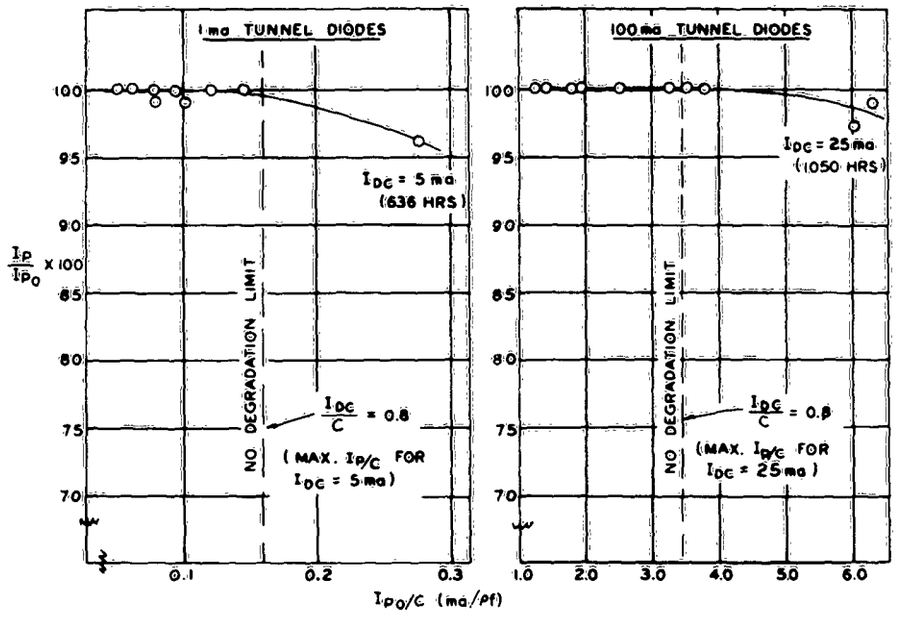


Figure 2-16. Application of Figure of Merit ($I_{DC}/C \leq 0.8$) for Operating GaAs Tunnel Diodes Under D-C Forward Bias with no Degradation (1)

(2) Dynamic Life Tests

Presently, nineteen 250-ma GaAs tunnel diodes are being operated at room temperature on a dynamic life test which simulates operation in the memory circuit. The test circuit, shown in Figure 2-17, provides that the diodes be driven at a 50-mc rate. After several hundred hours of operation, some of the diodes appeared to have degraded slightly. The changes have all been under 3% which is within the accuracy of the test equipment being used. This test should operate for several thousand hours, after which the significance of these small changes will be more clearly resolved.

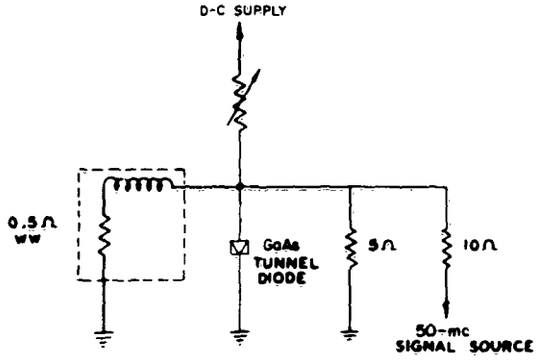


Figure 2-17. Dynamic Life Test Circuit (1)

(3) Oscillator Operation

It was reported in the last IRR that a tunnel diode operated for 500 hours in a stripline oscillator circuit at 92°C without degradation. A 65-ma diode has been operated without change in a 200-mc oscillator at 150°C for 200 hours. The I_p/C ratio for this diode is 2:1.

(4) Reverse Bias Operation

It has been previously reported that tunnel diodes do not degrade in the reverse direction. It has been found, however, that if sufficient current is passed through the diode the valley current will rise, and often the negative-resistance region disappears, leaving only an inflection point. Further, whereas the usual degradation is irreversible, it was found that operation of the diode in the forward direction essentially restores the original characteristics.

Table 2-12 shows a typical test in which the diode was operated at high reverse currents followed by forward operation. Full-wave rectified sinusoidal voltages were applied across the diode, and the values listed in Table 2-12 are the respective peak and valley currents.

TABLE 2-12
DEGRADATION OF GaAs DIODES DURING OPERATION IN THE REVERSE DIRECTION (CAPACITANCE 37 pf, R_s=1.13)

I_p (ma)	I_v (ma)	Comments
199	4.6	Initial values
196	4.4	after 3 seconds at 700 ma
193	4.4	after 3 seconds at 800 ma
195	4.5	after 3 seconds at 900 ma
202	65.0	after 3 seconds at 1 ampere
190	19	after 10 minutes operation just beyond valley
195	4.5	after 20 seconds operating at E_r

Observing an unencapsulated diode through a microscope while it was being operated in the reverse direction indicated an apparent melting of the alloy dot at the same time that a shift in the slope of the reverse characteristic appeared. This shift in the reverse characteristic normally accompanies the drastic increase in valley current. It may be thought that the process of melting results in a shunt conductance across the junction, but this cannot account for the observed recovery after operating in the forward direction. Surface effects might possibly account for these changes. Further work on this phenomena is necessary.

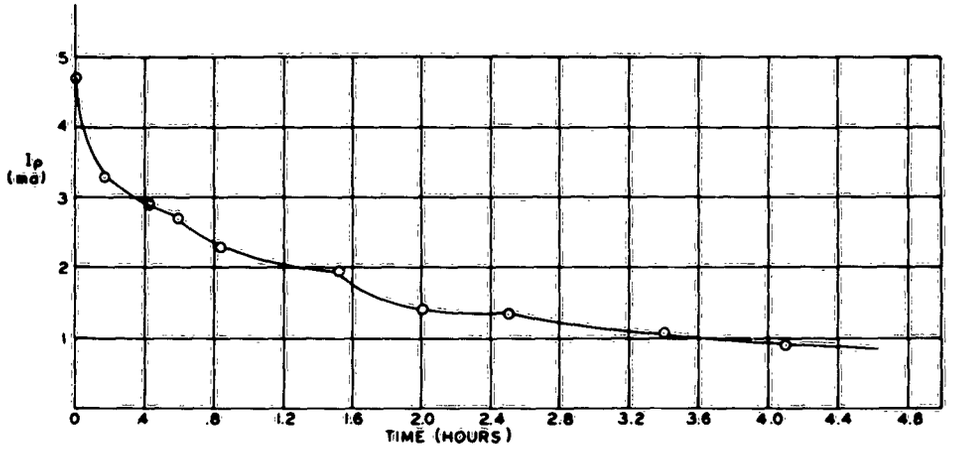


Figure 2-18. Degradation of 5-ma Germanium Tunnel Diodes (1)

(5) Degradation of Germanium Tunnel Diodes

A group of ten germanium tunnel diodes with I_p = 5 ma were operated at 100 ma forward current. The capacitance values ranged from 3.1 pf to 7.0 pf. These tunnel diodes degraded much in the same fashion as GaAs tunnel diodes when operated at E_F. The degradation depends upon I_p/C, being more rapid for diodes with higher speed ratios. Figure 2-18 illustrates a typical change in peak current as a function of time during degradation. A "fine" structure of somewhat scalloped appearance of the plot of I_p vs. time may be observed. This "fine" structure has also been observed in the degradation of GaAs tunnel diodes, and may be due to the changes in the non-uniform tunnel-current distribution through the junction.

Similar results have also been obtained with 50-ma germanium diodes operated at 200 ma forward current. A typical result is shown in Figure 2-19.

b. Effects of Diode Fabrication on Degradation

(1) Diodes With Sn/In Alloy Dots

During this quarter, the investigation of diodes made with tin/indium alloy dots has continued. Tunnel diodes were made with one zinc-doped crystal, using alloy dots whose composition varied from pure tin to 15% tin/85% indium. The forward voltage, E_F, varied with the alloy composition, but not monatonically. This is shown in Figure 2-20, where the data is corrected for series resistance.

The forward voltage of these diodes is also related to the peak-to-valley current ratio, I_p/I_v. Diodes with higher forward voltage also had higher I_p/I_v ratios, as shown in Figure 2-21. Since the valley current is attributed to excess current due to tunneling into the forbidden gap, this suggests that the current at the forward voltage E_F is also excess current, rather than minority carrier injection current.

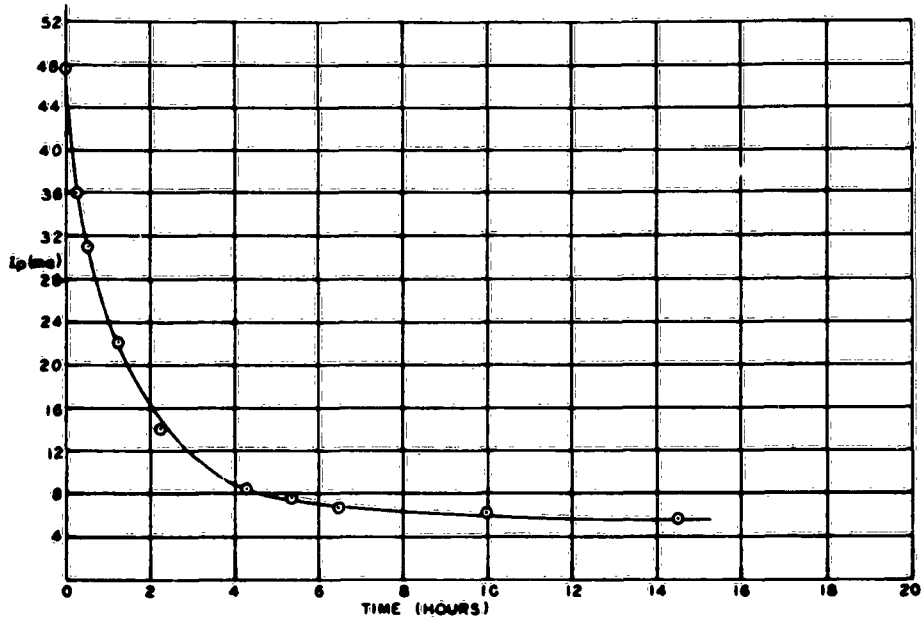


Figure 2-19. Degradation of 50-ma Germanium Tunnel Diodes (C_{VO}=8.15 pf, I_{DC}=200ma) (1)

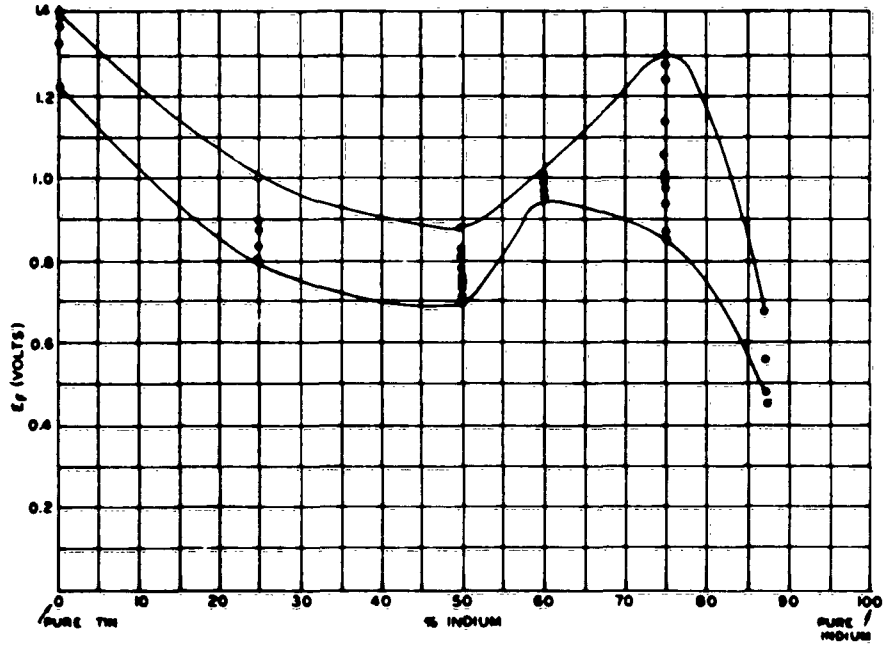


Figure 2-20. Dependence of Forward Voltage (E_f) on Alloy Dot Composition (1)

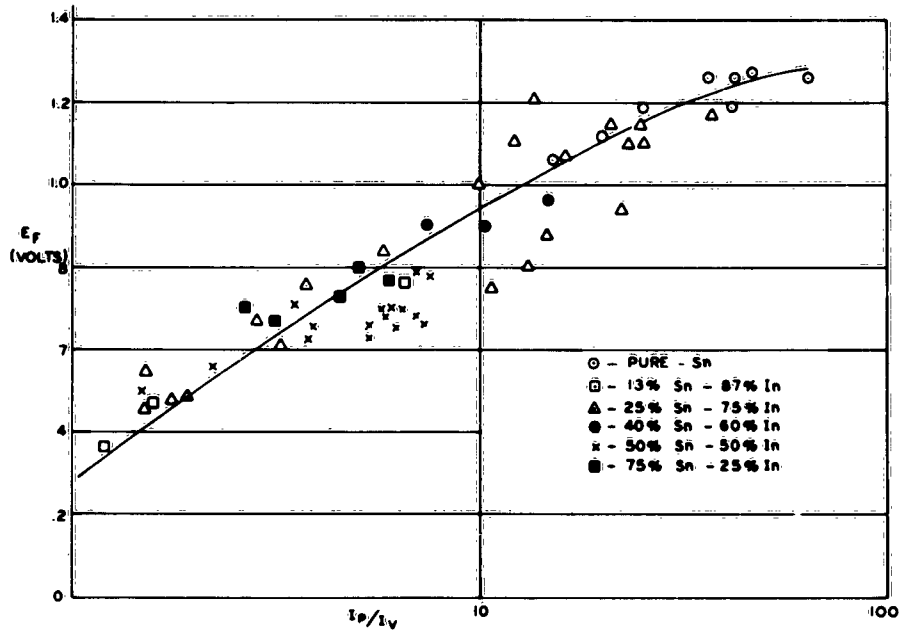


Figure 2-21. E_F vs. I_p/I_v for Different Dot Compositions (E_F Corrected for Series Resistance) (1)

Several diodes made with 75% indium-25% tin had electrical characteristics comparable to those made with pure tin dots. Life tests of both groups of diodes showed the ones with Sn/In dots to be far superior to the diodes made with pure tin dots. Figure 2-22 is a comparison between the peak current vs. time for one diode from each group. Both diodes had comparable and fairly high-speed ratios, and essentially identical forward voltages (i.e., identical power dissipation). (Note the difference in time scales in Figure 2-22). Diode No. In-40 degraded more slowly than No. Sn-10 by a factor of several hundred. Although the use of 75% tin alloy dots does not entirely eliminate the degradation, the improvement is notable. This approach is being pursued with the aim of improving the life characteristics still further and also obtaining better control with this process.

(2) Copper-Free Gallium Arsenide

Tunnel diodes were made from Zn diffused crystal which was "leached" with KCN (reported in the last IRR). Typical I_p/I_v ratios are about 2.0 and consequently the values of E_F are low, ranging from 0.40 to 0.76 volt. The control wafer, diffused but not leached with KCN, also had relatively low values of E_F, but was better in this respect than the leached units. These values range from 0.84 to 1.04 volts. Both sets of tunnel diodes, with 100-ma peak currents, were placed on a life test at 100 ma, and later at 200 ma forward current. The leached diodes did not fail as rapidly as the control unit but the total power dissipation is somewhat less for the leached diodes.

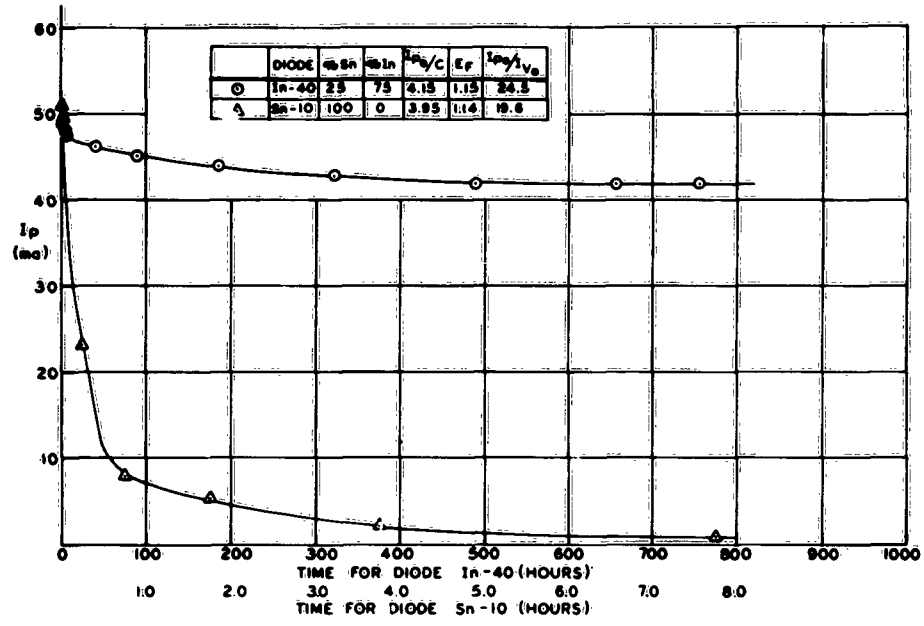


Figure 2-22. I_p vs. Time for Two Diodes (1)

Figure 2-23 shows the relative failure rates for two typical diodes. Further experiments of this type will be conducted in order to determine whether or not the apparent improvement in degradation rate is real, and to see if better peak-to-valley ratios can be obtained.

In addition, a wafer of GaAs has been Zn diffused in the radiation furnace described in the last IRR. Diodes now being made from this wafer will be put on life test.

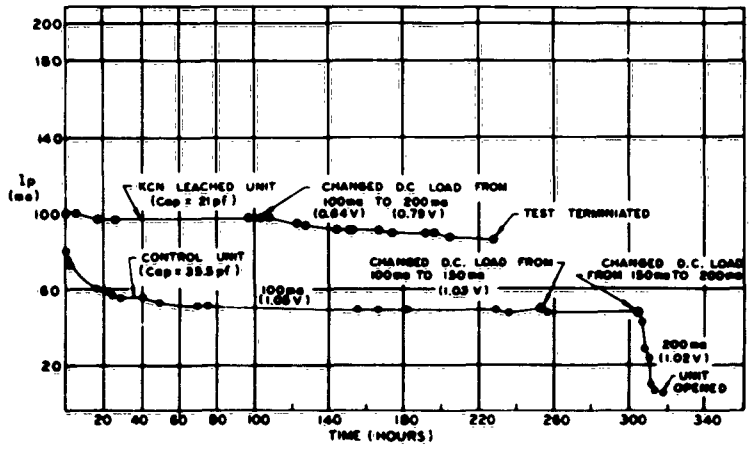


Figure 2-23. Effect of Leaching on Tunnel Diode Degradation (1)

c. Degradation Mechanism

In the previous IRR, a model was proposed to explain the degradation of GaAs tunnel diodes. The principal feature of that model was that the recombination process played an important role in the degradation mechanism. It was thought that this process involved the recombination of injected minority carriers with majority carriers through recombination centers believed to be copper. It was further believed that energy transferred to the recombination center was sufficient to cause a significant fraction of centers to change from substitutional to interstitial copper. The positively charged interstitial copper then diffused rapidly towards the junction, where it formed an ion pair with the negatively charged zinc acceptor, thus widening the junction depletion layer.

Some experiments have been performed since then which suggest that, for diodes with peak-to-valley current ratios of only 15 or less, this model should be modified in some respects. It now appears that the current under which degradation occurs in these relatively low-ratio diodes is excess current, rather than minority carrier injection current. This was first suggested by the dependence of forward voltage on peak-to-valley current ratio (see Section B. (1)). To verify this, the forward I-V characteristic of a tunnel diode with $I_p/I_v = 10$ was measured at different temperatures. The current was found to be an exponential function of voltage only, as shown in Figure 2-24. Note that the slope of log I vs. V is independent of temperature. This is characteristic of excess current, whereas injection current would show steeper slopes for lower temperatures.

In view of this, some details of the model have been changed. The major feature, however, is still retained. Excess current involves the tunneling of electrons into the forbidden region, and subsequent recombination with a hole in the valence band. This can occur through recombination centers in the depletion layer, or the dopant atoms themselves may act as recombination centers. In either event, the recombination energy associated with the excess current probably plays an important role in the degradation mechanism.

For diodes with higher values of I_p/I_v, thermal injection current is comparable to or larger than the excess current at forward bias conditions which cause degradation. The model described previously therefore still applies to these diodes.

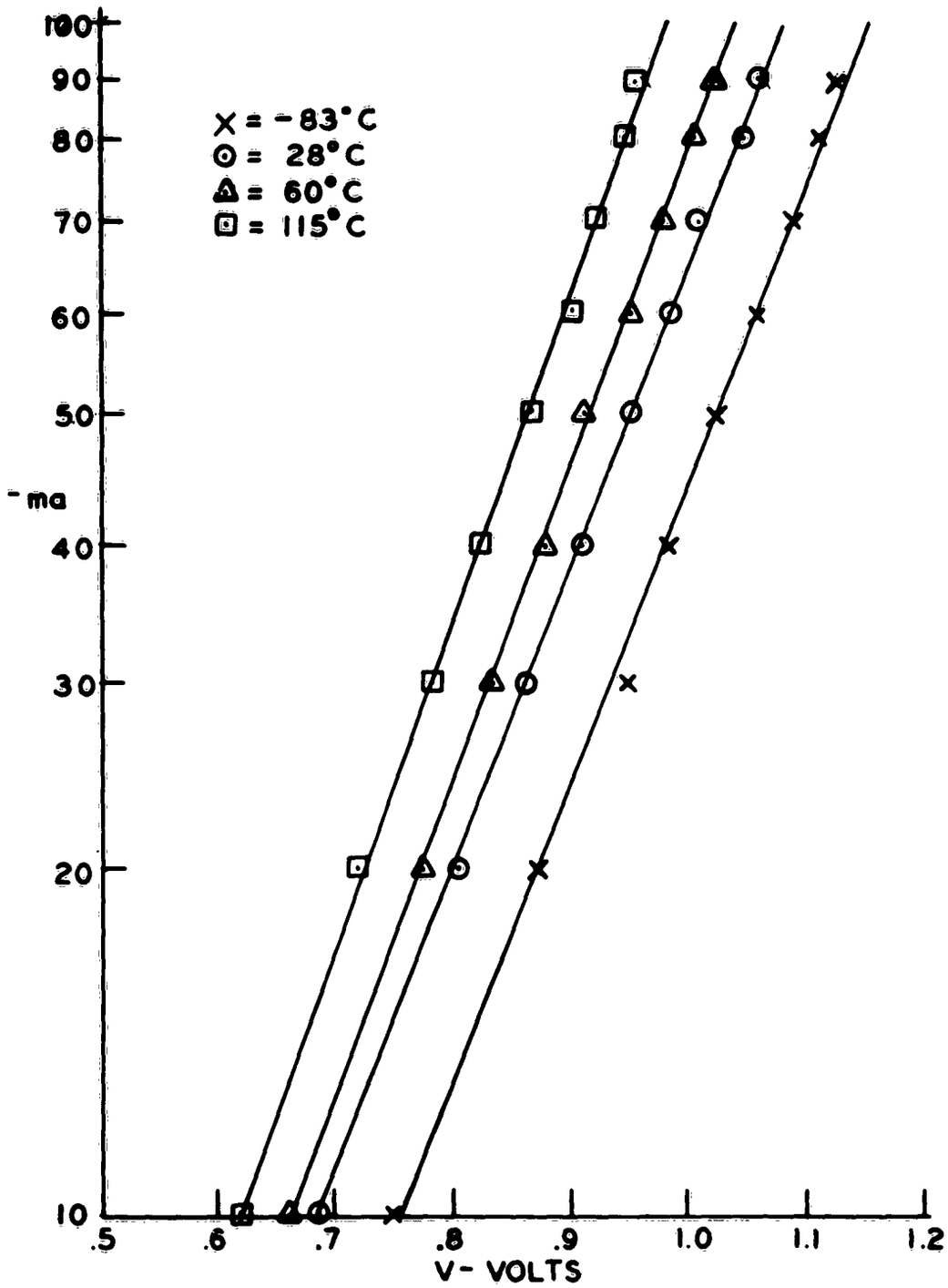


Figure 2-24. Current vs. Voltage for GaAs Tunnel Diode With $I_p/I_v = 10$ (Data Corrected for Series Resistance) (1)

III. PROGRAM FOR NEXT INTERVAL

Production run of germanium tunnel diodes and tunnel rectifiers needed for the logic subsystem will continue. A basic program on tunnel diode crystal material will be initiated.

High-speed tunnel diodes ($I_p/C \geq 10:1$) and low capacitance tunnel rectifiers will be supplied to the Laboratories Division, for use in the High-Speed Subsystem.

Development will continue of the solution alloying SiO mask technique. Evaluation of the beam-type screen connector will continue.

Low dielectric constant insulating materials will be investigated for use as a package insulator, and the new package design will be evaluated. More precision life tests will be started and the large-scale precision life test program will be put into operation.

Electrical specifications will be determined and deliveries of GaAs tunnel diodes (fabricated by solution alloying process) will be made. Life tests, both dynamic and static, will be started for the GaAs solution alloyed diodes. Investigation will continue of Sn/In dots, and on the effect of copper removal on GaAs tunnel diode life and electrical characteristics.

Chapter 3. LOGIC CIRCUIT DEVELOPMENT

I. SUMMARY

An improved version of the magnetically coupled flip-flop described in a previous report has resulted in a circuit with improved load line characteristics and low recovery time. As before, the problem of resetting such a circuit still exists; however, a solution is proposed which requires further refinement.

Chapter 3. LOGIC CIRCUIT DEVELOPMENT

I. PERSONNEL

The following personnel contributed to this phase of the project during the eleventh quarter.

R. H. Bergman
H. Ur

II. DISCUSSION

LOW RECOVERY TIME, COMPLEMENTING, MAGNETICALLY COUPLED FLIP-FLOP

This circuit is an improved version of the tunnel diode complementing flip-flop described in IRR-4A p. 3-15. The circuit as revised is shown in Figure 3-1. The combination of the clamp diode and R_1 resulted in an improved non-linear load line as shown in Figure 3-2.

This circuit has the following advantages over the previous version:

(1) Lower recovery time

(2) Improved level sensitivity (load line horizontal at point A, Figure 3-2)

(3) Improved loading capability (load line vertical at point B, Figure 3-2)

The circuit operates as follows: Assume that the circuit is in the state of TD_1 high and TD_2 low. A positive pulse is applied to TD_2 causing it to switch. This will induce a voltage on the other side of the transformer which will switch TD_1 to the low state.

For convenience, the circuit was tested in the triggered mode with both inputs connected together and fed by a pulse train. In this mode of operation, when a pulse is applied to the input only the low side is affected. The high side is unaffected as it is blocked by the directional diode. Waveforms keyed to points in Figure 3-1 are shown in Figure 3-3.

One difficulty with this circuit, as was with the older version, is that if the circuit happened to be in the unpermissible mode (both sides being in the high state), an input pulse could not switch it to the proper state. A proposed solution is the application of a pulse on the winding of the transformer. Because of the polarity of the windings, this pulse will produce a positive trigger in one diode and a negative in the second, and consequently tend to switch one diode high and the other low. This reset scheme was tried and was found to work, however, somewhat erratically. Thus, further investigation is needed to find the proper conditions of operation. It is believed that this effect may be due to two sources: first, the reset pulse was too

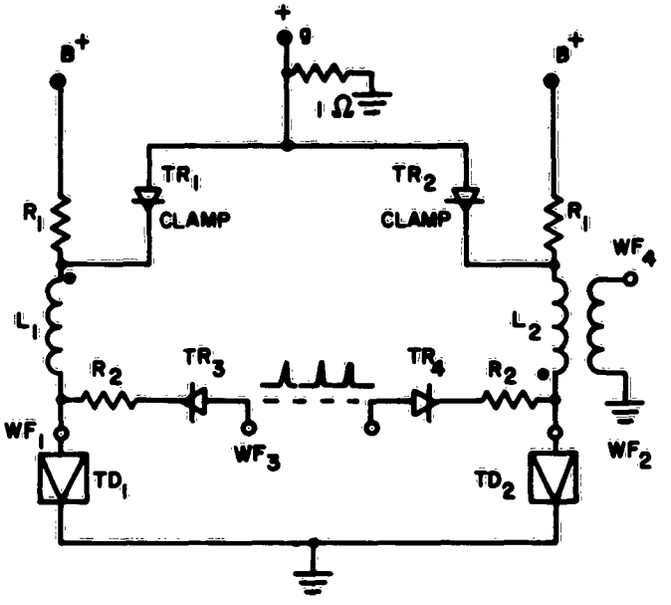


Figure 3-1. Magnetically Coupled, Complementing Flip-Flop Circuit (1)

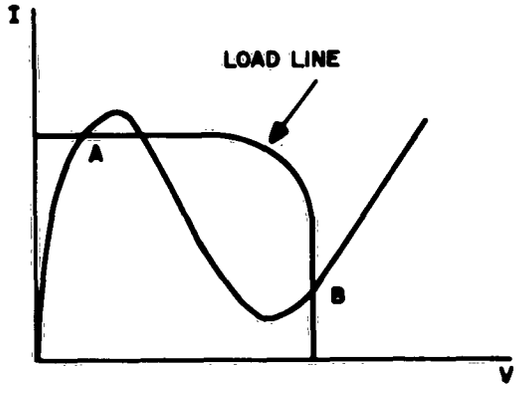


Figure 3-2. Operating Conditions for Circuit of Figure 3-1 (1)

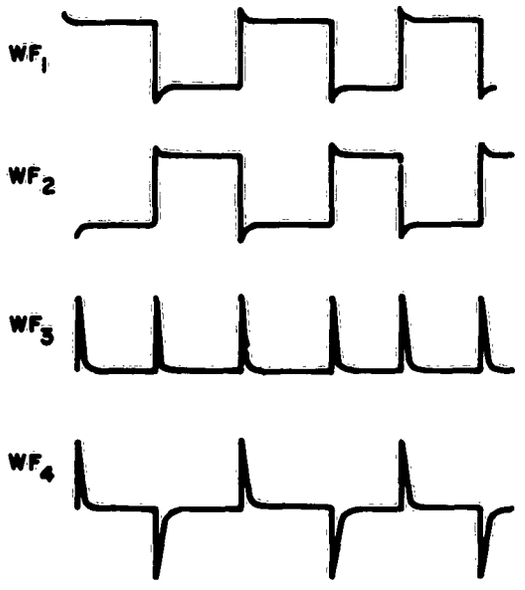


Figure 3-3. Waveforms from Circuit of Figure 3-1

long and the transformer acted as a differentiating network producing an inverted polarity pulse at the trailing edge; secondly, a resonant condition of the inductances, stray inductances and capacitance produced overshoots.

The circuit was operated using Q2 cores with input frequencies of up to 80 mc. It also was operated with one core of hexagonal material obtained from the Laboratories Division. Despite the very small dimensions of this core, it produced too much inductance and prevented a fast operation. It appears, however, that this material has, with respect to Q2, superior high-frequency response and μ values. Thus, it is felt that with proper size hexagonal cores, higher frequency operation could be obtained.

Chapter 4. FABRICATION

SUMMARY

A cable bender suitable for both bending the cable required for the test vehicle and for studying the bending properties of miniature cable was constructed.

Design of a wafer holder for the test vehicle was chosen and holders were obtained.

Several useful tools to aid in wafer assembly were constructed.

Several advanced development designs of wafers and frames were proposed.

Chapter 4. FABRICATION

I. PERSONNEL

The following personnel contributed to this phase of the project during the eleventh quarter:

I. Abeyta
F. E. Brooks
D. R. Crosby
M. E. Ecker
R. J. Fradette
A. M. M. Hoque
H. R. Kaupp
W. J. Lipinski
E. Luedicke
H. Reinig

II. DISCUSSION

A. COAXIAL CABLE AND CABLE FORMING TOOL

A coaxial cable forming tool was designed and constructed, as shown in Figures 4-1 and 4-2. Using this device, coaxial cables having .035- and .027-inch outside diameter were formed through an arc of 180 degrees with a minimum forming radius of .078 and .048 inch, respectively. Further forming studies will be pursued with miniature coaxial cable having shields of various materials and outside diameters as small as .010 inch.

Figure 4-1. Cable Forming Tool (u)

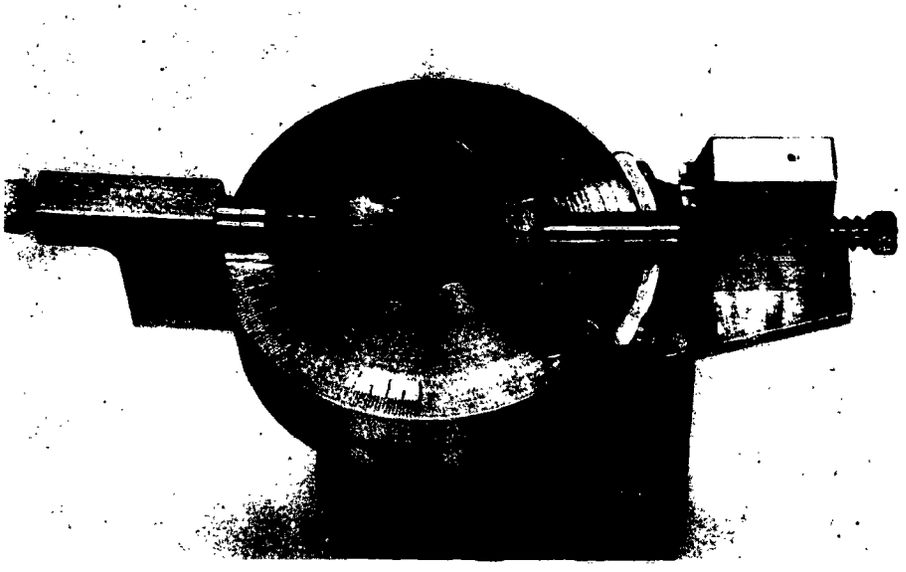


Figure 4-2. Detail of Cable Forming Tool (1)

The tool illustrated in Figure 4-1 is operated by rotating the forming spindle from the underside of the forming table until the desired forming radius is indexed into position. The four-jaw collett is opened by depressing the collett knob, permitting loading of the cable to be formed. With the forming die in a retracted and forming start position, the collett assembly is rotated until the coaxial cable is nested in the groove of the forming spindle. Then the forming die is released by rotating the knob and advanced until it is nested about the coaxial cable. Rotation of the die retracting knob about the periphery of the forming table shapes the coaxial cable to the desired arc.

1. Cable Handling

A loopback method of cabling for interconnecting the circuitry on logic wafers seems to be the most attractive at this time. It offers uniformity of forming pattern, good distribution of cable for connection to wafer contact points, ease of coding and a minimum number of catalogued parts.

The coaxial cable will be color coded with six color bands: two color bands to indicate distance between the connection points along the bottom edge of the wafer, two color bands to indicate the distance between wafers to be connected, one color band to indicate the number of rows of wafers between connections, and one color band to indicate the cable's characteristic impedance. All coaxial cables used to wire the frame assemblies will be preformed and color coded as described. Since this wiring approach will require some stacking of cables, it is desirable to control the order of wiring. This will be achieved by using a series of overlays representing portions of the wiring schematic and organized such that the wiring is done in a particular sequence.

2. Cable Connectors

A multiple cable-to-cable connector using soldered connections was developed. This connector, shown in Figure 4-3, is presently undergoing test to determine the crosstalk and reflections it produces.

B. OPEN FRAME

The open frame design has been revised so as to be comprised of "I" beams held together by interlocking crossbars. The crossbars incorporate a frame connector for external connections. The connector was also revised to allow the frames to be inserted vertically into the subsystem rather than slid in horizontally. All connections in the connector will be on top of the frame and easily accessible as test points.

The frames can be made in various sizes accommodating 15 to 75 wafers. The variation in size is accomplished by using appropriate length crossbars. The "I" beams are of fixed length, holding 15 wafers.

Figure 4-4, right-hand side, shows a frame and several holders being constructed for the test vehicle. An advance development frame with improved holders is shown on the left side of the figure.

The low-impedance transmission lines are inserted into the "I" beam of the frame using a low melting temperature solder and oven heating. A tinned copper strip with welded tabs is then soldered to the line to allow connection to the wafers.

Figure 4-3. Multiple Cable-to-Cable Connector (U)

Figure 4-4. Open Frames with Holders (u)

C. WAFER HOLDERS

The wafer holder design which has been adopted uses a solder connection to both the outer and inner conductor of the coaxial cable. Laboratory tests showed that the components were not damaged in the soldering operation.

A study was made to provide a solderless connection from the holder to the cable, and various type holders were designed and constructed. Several of these holders are shown in Figure 4-5. Although these holders were acceptable, the soldered connection appears more reliable and simple.

The adopted wafer holder incorporates a thermal barrier in the form of a slot to facilitate the soldering of the coaxial cable. This slot restricts the heat transfer away from the connection points. Figure 4-6 shows the wafer holders constructed for this thermal study.

D. SOLDERING TOOLS

1. Template

The feasibility of soldering all diodes onto the wafer in one operation is being investigated. A brass template having slots into which diodes are inserted in proper location was constructed, as shown in Figure 4-7. After the diode tabs and the wafer circuit have been tinned, the template is filled with diodes and positioned onto the wafer. Heat is applied to the underside of the wafer and all diodes are soldered to the wafer. The initial results were promising and improvements on the template design will be made.

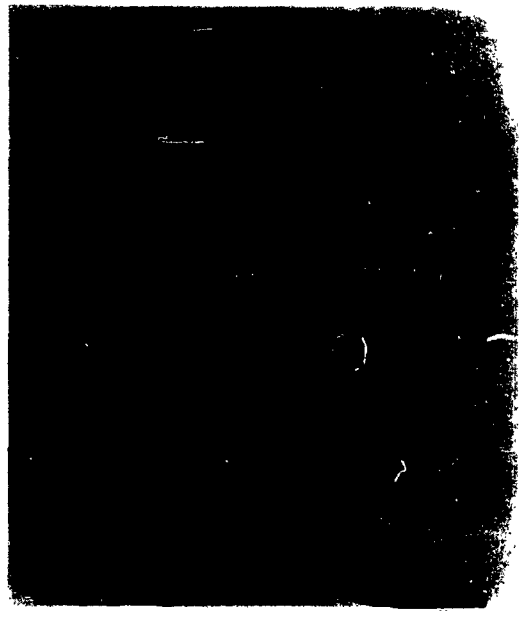


Figure 4-5. Wafer Holders with Solderless Cable-Sheath Connections (1)

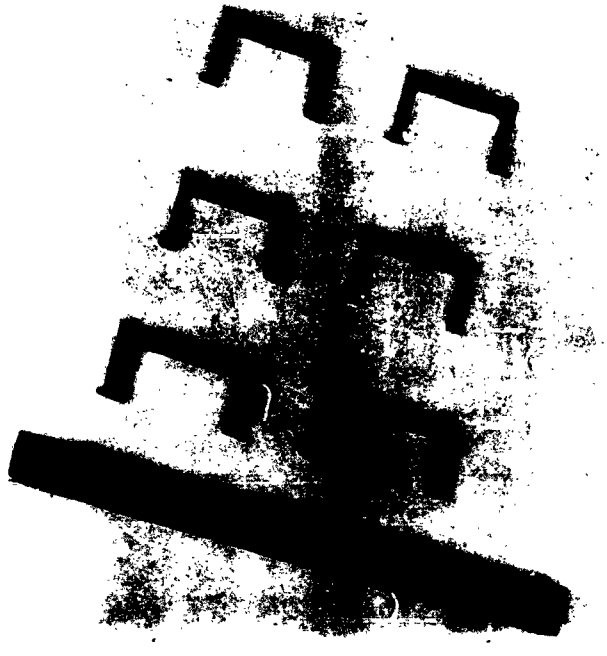


Figure 4-6. Wafer Holders with Soldered Cable-Sheath Connections (1)

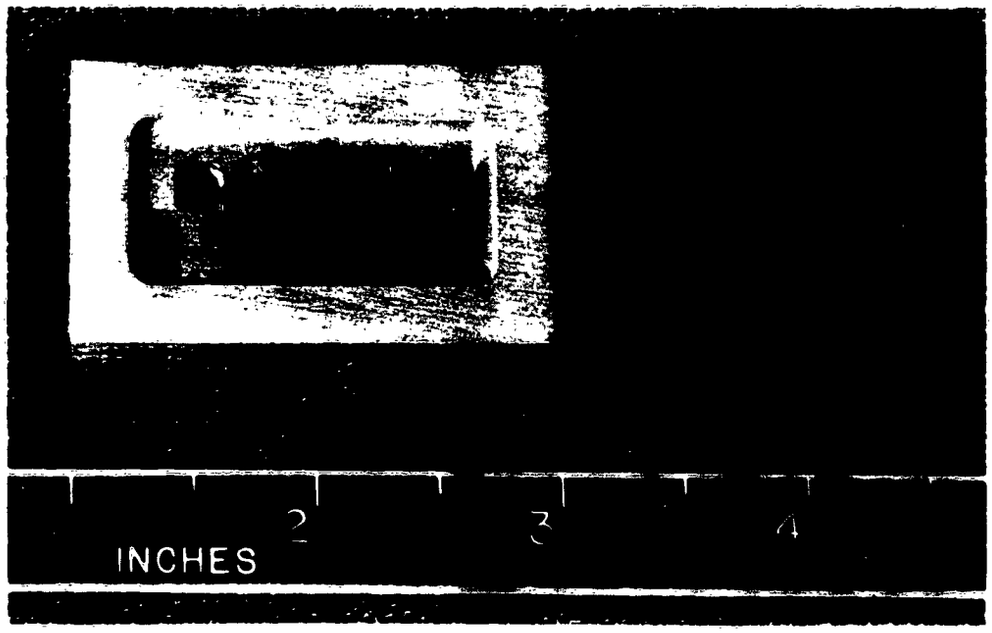


Figure 4-7. Tunnel Diode Soldering Template with Wafer (u)

2. Tweezers

The tips of several sets of tweezers were modified for use in various soldering operations. The set shown in the center of Figure 4-8 holds a tunnel diode while it is being soldered. The tweezer heads provide a heat sink to draw the heat away from the diode. These heads are designed so that no pressure is applied to the diode center while being held. Results using these tweezers were satisfactory and several sets are now in operation. A second set of tweezers for holding rod resistors was designed. This set is shown on the left of Figure 4-8. The resistor is held on its entire diameter to prevent damage to the film. The first set had teflon tips which performed well but deteriorated under prolonged use. A second design uses aluminum tips as shown on the right of the photograph (Figure 4-8).

3. Soldering Irons

A soldering iron was designed for soldering both ends of rod resistors in one operation. As seen in Figure 4-9, left-hand side, the tip of a standard iron was milled to provide a split tip so that both ends of a resistor could be soldered at the same time. The results were satisfactory and several irons have been similarly modified. A split tip iron for soldering coaxial cables to the holders has been constructed as shown on the right-hand side of Figure 4-9.

E. WAFER CONNECTOR

A miniature wafer connector was designed, and a scaled-up model is being constructed for further study. Details of this connector are illustrated in Figure 4-10.

Figure 4-8. Special Tweezers for Tunnel Diodes and Resistors (s)

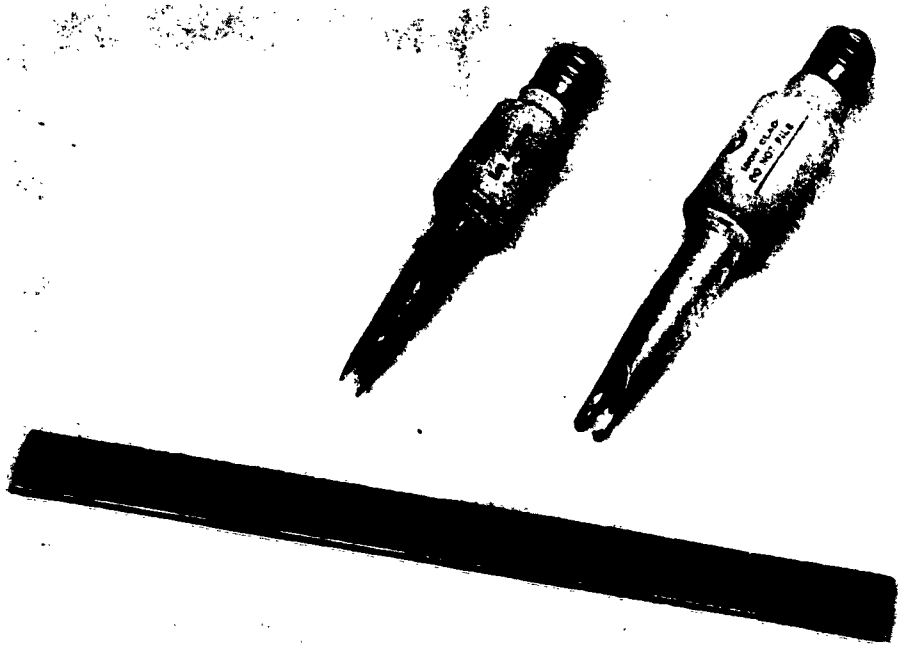


Figure 4-9. Split Tip Soldering Irons for Resistors and Miniature Cables (s)

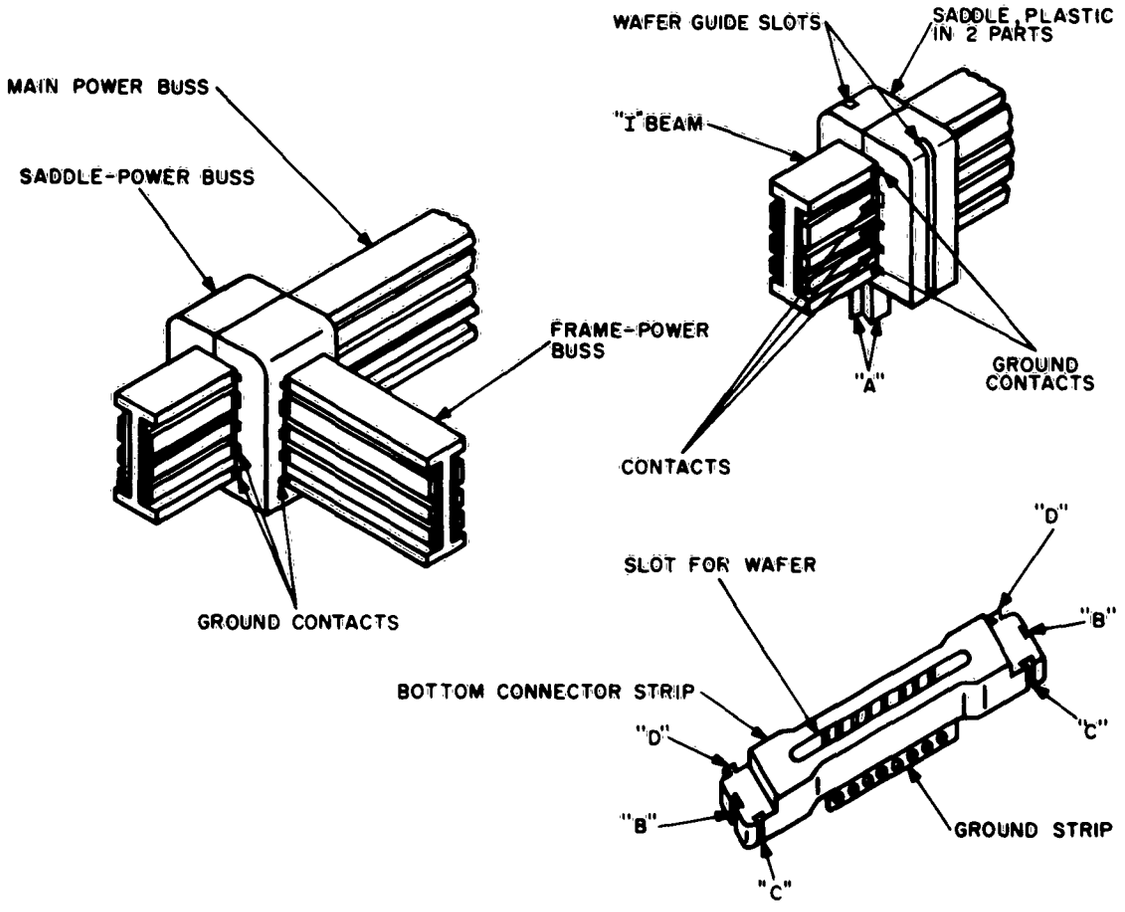


Figure 4-10. Plug-In Wafer Connector (1)

Contact between the pads on the wafer and the interconnecting coaxial cable or low-impedance power supply lines is made with a gold plated beryllium copper spring member. The strip connector assembly has two rows of contacts placed along its length. One row is for making contact to the ground surface of the wafer, and the other row is for making contact to the input and output pads on the wafer. Both rows of contacts terminate on the underside of the connector strip where the coaxial cable is attached. The coaxial cable is passed through a hole in the grounding strip and soldered. The center conductor of the coaxial cable is positioned on the contact and soldered. The grounding strip contact is folded around each pad contact to achieve shielding between pad contacts. Connection between the wafer and the low-impedance power supply line is made by use of the saddle connector. The saddle connector is designed such that spring contacts, located on the rear face and terminating in the wafer guide slot, make contact with the various low-impedance power supply lines and two grounding points when the saddle connectors are attached to the "I" beam supporting

the power supply lines. After the saddle connectors have been attached to the "I" beams, the bottom portions of the saddle connectors are inserted into the grooves located at each end of the strip connector. When the wafer is inserted into the guide slots of the saddle connectors and pushed down until the bottom edge of the wafer is fully seated in the slot of the strip connector, all the spring contacts are sufficiently deflected so as to provide satisfactory contact. This construction permits assembly of any number of connectors in any arrangement desired. When connectors and "I" beams are assembled, they form their own supporting structure. Also shown in Figure 4-10 is a connector based on the design of the saddle connector that would permit connecting two sets of adjacent low-impedance power supply lines to one low-impedance power supply line.

Another approach to the design of a plug-in wafer connector is shown in Figure 4-11. Here the means for making contact between the wafer and the coaxial cable or low-impedance power supply is a cylinder of resilient-mesh contact material. The resilient-mesh contact is an intricately woven gold-plated copper wire about 2 mils in diameter that is formed into a cylindrical shape. Contact is made by compressing the material between surfaces to be connected. All contacts terminate in the wafer slot and the "I" beams supporting the low-impedance power supply lines are sandwiched between the connector's sides. Further design considerations are necessary before a prototype unit of this wafer connector can be constructed.

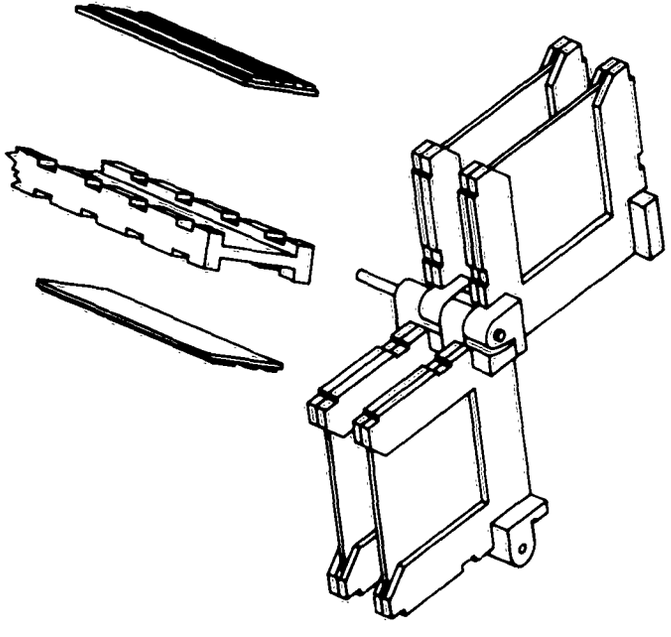


Figure 4-11. Hinged Wafer Assembly (o)

F. NEW SUBASSEMBLY SCHEME

A new type of subassembly is under investigation with the aim being to provide easier access to the wafers and to facilitate the wiring of the low-impedance power buses to the wafer. It consists of a multi-layer plane with cut-outs into which the double-face wafers are inserted. The signal wires, located in channels at the bottom of the multi-layer plane, are connected to the "fingers" of the double-face wafer. As shown in Figure 4-12, the power bus lines are connected to the face of the wafer with taps originating from one of the layers of the multi-layer plane.

1. Double-Face Wafer

The material from which the double-face wafer is manufactured is shown in Figure 4-13. It has a central section which consists of a conductive material, such as copper or aluminum, with a thickness of 0.060 inch to 0.1 inch. An insulating material, e.g. teflon, with a thickness of 0.010 inch to 0.020 inch is secured to each side of this central section. The outside of this dielectric material is covered with a thin layer of printed circuit copper.

The laminating process may be carried out by a heat, pressure or adhesive process; the laminated material can then be stamped or machined to the desired shape.

The configuration which was chosen for this subassembly is shown in the upper portion of Figure 4-14. The "feet", F, serve as electrical ground connections as well as heat sinks between the wafer and the multi-layer plane.

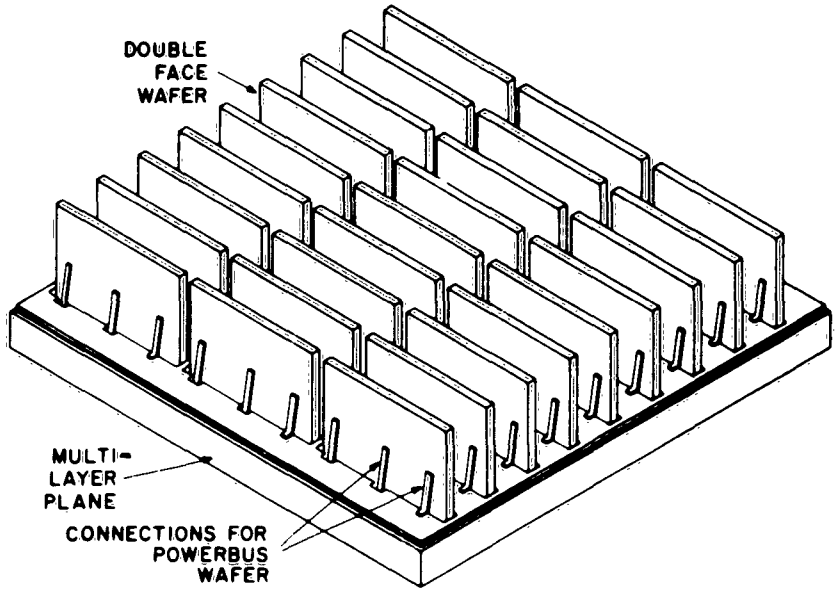


Figure 4-12. Subassembly Using Multi-Layer Frame (1)

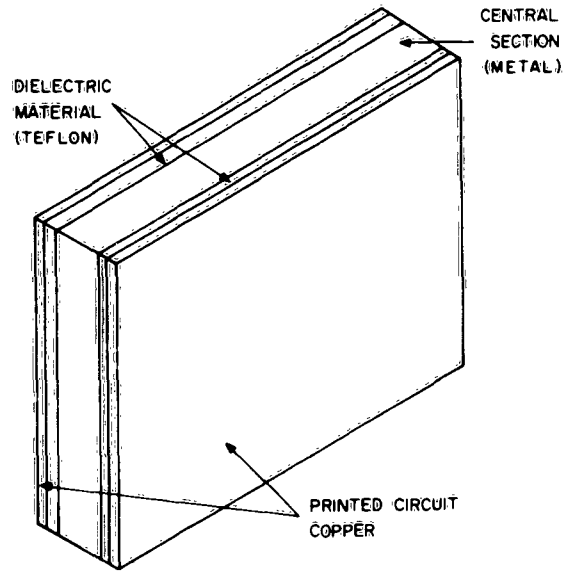


Figure 4-13. Double-Face Wafer Material (1)

The "fingers" B, are the input and output terminals for the signal connections. The printed circuit pattern is etched on each side of the wafer using a photo etch or silk screen method.

Holes (H) are drilled or punched through the wafer, and the components are mounted in the holes and secured to the printed circuitry on both sides of the wafer.

The printed circuitry on both sides of the wafer can be coated with a thin layer of insulating epoxy and then with a coat of conductive paint. The final coat acts as a shield for the circuitry on the wafer. This complete metal enclosure of the components results in a reduction of stray inductance and spurious coupling, and permits higher frequency operation.

2. The Multi-Layer Plane

The construction of the multi-layer plane is shown in the lower portion of Figure 4-14. This unit is capable of transmitting three separate power bus lines. Also, it can accommodate numerous signal wires by using the channel wiring configuration at the underside. The plane is fabricated by alternately laminating sheets of copper and teflon. The sheets, G, are the ground planes and are connected with pins to the grounded channel wiring plane CW. Sheets T are teflon and sheets P are the copper transmission planes. The thickness of the teflon sheets, T, may be adjusted to obtain various values of impedances for transmission planes P.

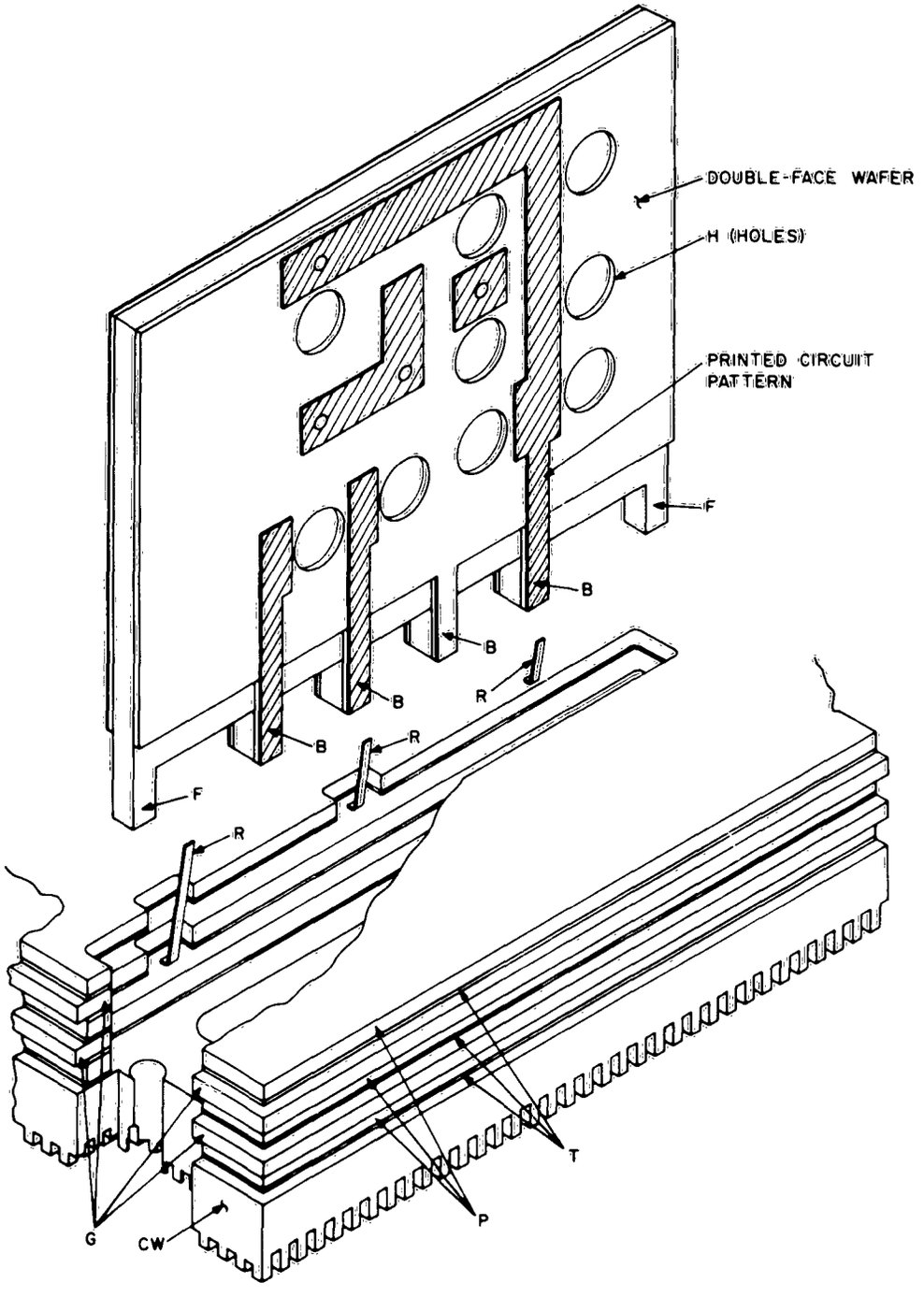


Figure 4-14. Double-Face Wafer and Multi-Layer Frame (4)

Notches are cut into the planes to allow the wafers to be inserted. The tabs, R, are connected to the different transmission planes, P, and serve as connections to the low-impedance power bus from the plane to the wafer.

Fabrication of a prototype of this construction is in process.

G. WAFER TEST FIXTURE

A wafer test fixture was designed and constructed for testing a .775 x .400 x .020-inch wafer for channel wiring application. This fixture is shown in Figures 4-15 and 4-16. Since the completion of this test fixture, the wafer size has been doubled and the channel wiring technique was abandoned. This fixture will now be used for evaluating the resilient wire mesh contact.

H. FEASIBILITY SUBSYSTEM WORK

Design work was begun on subsystem construction. The subsystem will be composed of six open frames of varying sizes, integrated into a main frame. It is proposed that each open frame be removable from the main frame and tested in its own test fixture.

Figure 4-15. Wafer Test Fixture (+)

I. MEMORY CELL PACKAGE

A molded plastic package to ho.. two memory cells was developed, as shown in Figure 4-17. This package holds two tunnel diodes, two tunnel rectifiers and two resistors.

Figure 4-16. Detail of Wafer Test Fixture (c)

III. PROGRAM FOR NEXT INTERVAL

Thermal properties of wafer and frame assemblies will be studied. Improved assembly tools for the tunnel diodes and resistors will be developed. Simpler frame-to-frame connectors will be developed. A main frame and cooling system for the test vehicle will be designed.

A quick removable wafer employing spring finger contacts will be developed.

The advanced development frame and wafer designs will be evaluated, and mechanical properties of 10-mil diameter cable will be studied.

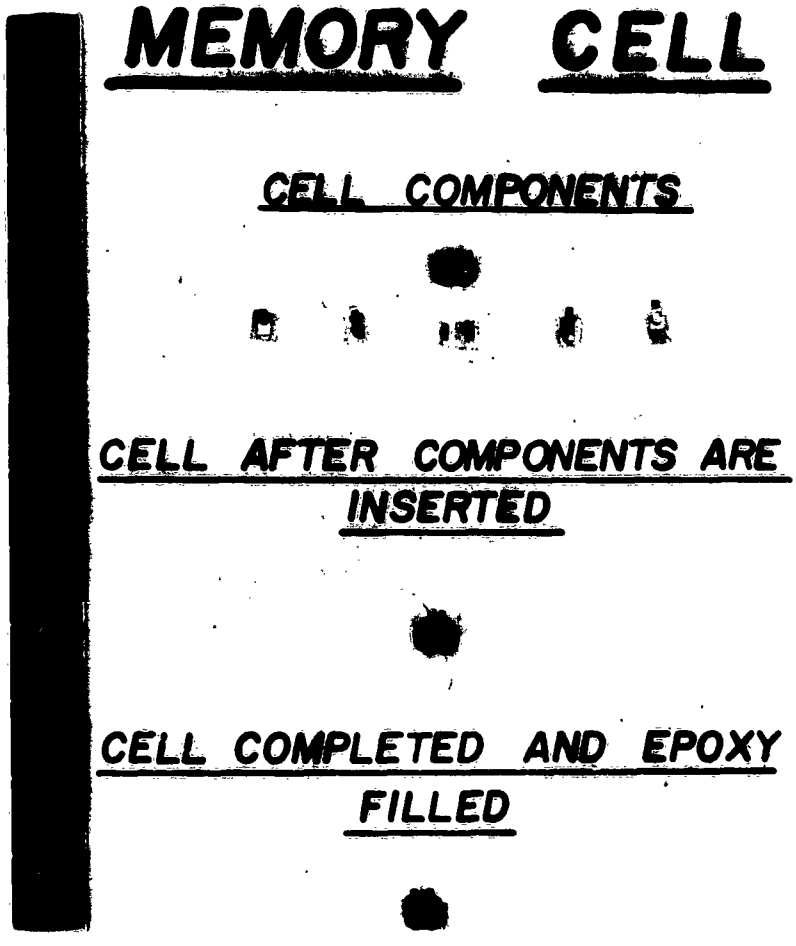


Figure 4-17. Memory Cell Package (1)

Chapter 5. TASK III (HIGH-SPEED SUBSYSTEM)

SUMMARY

The goals of Task III have been examined and it has been decided that to meet them, it is necessary to have a single-stage tunnel diode logic gate fabricated in an extremely small, three-dimensional package. It has also been decided that the gates will have to be made such that they can be individually adjusted to tight tolerances.

Some special soldering techniques are being studied, but at present conductive epoxies are being used to assemble the miniature, tunnel-diode circuits.

Several tunnel-diode logic gates have been constructed in packages .5 inch x .5 inch x .2 inch. These have been operated at repetition rates in excess of 700 mc and with stage delays of less than .5 nanosecond.

Some special components for Task III circuits have been made during this quarter. These include miniature inductors, hexagonal ferrite transformer cores, and low-dissipation non-linear loads made by plating a metal film directly over the tunnel-diode junction.

Work is well under way to provide instrumentation for Task III. An ultra-high-speed sampling oscilloscope is nearing completion. High precision measuring equipment is also nearly complete for measuring tunnel diode parameters to well under one percent.

Chapter 5. TASK III (HIGH-SPEED SUBSYSTEM)

I. PERSONNEL

The following personnel contributed to this phase of the project during the eleventh quarter:

G. A. Brown
L. S. Cosentino
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II. DISCUSSION

A. INTRODUCTION

The goal of Task III is to demonstrate the operation of tunnel diode logic circuits at higher speeds than are planned for the subsystems being constructed on Task II-A. The specific goal calls for the construction and test of a 40-gate, 0.4-nanosecond logic subsystem using circuits closely related to the circuits being used for Task II-A. The work during this quarter has been concentrated on formulating a reasonable approach to the Task III goal which can be carried out within the contract time period.

Certain ground rules which appear necessary have been established; some fabrication techniques have been developed and others are being investigated; some circuits have been conceived and tested; special components have been designed and fabricated; and instrumentation and component measurement techniques are being established.

B. GENERAL

Presently available tunnel diodes switch in 0.1 nanosecond or less and yet it is difficult to achieve stage delays of less than 1 nanosecond with tunnel diode logic gates. Tolerances are the chief cause of this difficulty. It has been found that to operate tunnel diode logic gates from a common power supply bus under worst-case tolerance conditions, two or more tunnel diode stages must be cascaded to achieve useable fan-in and fan-out. Cascading stages not only increases the switching time but also increases the physical size of the gates, since more components are required, and consequently increases the propagation delay. Faster tunnel diodes alone will not make the Task III goals attainable. It is necessary to obtain a single-stage tunnel diode circuit which can be constructed in a physically small package and made to operate reliably. Therefore, only single-stage circuits are being considered. To satisfy the requirement that the Task III circuits be of the same basic type as those being used on Task II-A, only d-c powered monostable and bistable circuits are being considered.

It is not likely that a circuit of this type will be found which has greatly relaxed tolerances compared with circuits presently known. Hence, emphasis is being placed on techniques for achieving close tolerances. Individual component adjustment is being considered as is individual power supply adjustment.

Inversion, which is required for resetting bistable circuits, is a major problem since the presently known circuits have long recovery times and therefore low repetition rates. Here again, single-stage circuits are required to meet the Task III goals. One approach being considered is the use of transformers made from a new hexagonal ferrite material. A costly but feasible alternative is the use of double-plane logic.

To keep the propagation delays within the Task III limits, it is necessary that a major part of the effort be directed toward development of packaging and fabrication techniques. Three dimensional packages, similar to those previously adopted for the balanced pair, are planned. Logic terminals will all be on one face of the package with power supply terminals being on the opposite face. Methods of reducing circuit power dissipation are also being explored since the high component-packing density will reduce the permissible dissipation.

In summary, the following ground rules have been adopted for Task III:

(1) Single-stage d-c powered monostable and bistable circuits

(2) Individual circuit adjustment to achieve tight tolerances

(3) Low power dissipation

(4) Smallest possible three dimensional packaging

C. FABRICATION

Integrated fabrication or the simultaneous fabrication of several components as a single unit, although obviously the most attractive approach on a long-range basis, is not a practical approach for Task III. The present low yields obtained in the manufacture of tunneling devices would make the yields of integrated devices infinitesimal. Therefore, the fabrication of circuits for Task III will be based on the assembly of individual components in miniature, three-dimensional packages. Logic terminals will all be on one face of the package and these logic faces will all be in a plane. Interconnection will be in the plane or in the space immediately above the plane. To keep internal propagation delay to a minimum, all components through which the signal must propagate will be kept as close to the logic terminal face as possible. It is planned to keep the area of the logic face of the package under .1 inch^2 and the total package volume under .05 inch^3. Several circuits have been constructed in packages of this size using the present-size tunneling devices. When smaller tunnel diodes are available, even smaller packages may be possible.

The principal problem in constructing circuits of this size is the means used to join the components to one another electrically and mechanically. Conventional soldering and welding techniques cannot be used. Three approaches are being explored.

Various conductive epoxies have been used with good success to construct experimental circuits. The only disadvantage in using epoxies is that once they have cured it is impossible to disassemble the circuit without destroying the components.

Another approach is to use low-temperature solders. Dots of this solder are placed between components and then the circuit is heated in an oven until the solder flows. For this method, suitable solders and fluxes must be found and special jigs will be required to hold the components while they are in the oven. This approach is being investigated, but as yet there are no results to report.

A third approach employs the phase transformation of an alloy of gallium and gold. In a recent publication[1], Harman described the use of certain gallium-gold alloys which initially have a low melting point but which undergo a phase transformation and subsequently have a much higher melting point. An experiment was performed to see whether simple gallium plating on gold surfaces pressed together would give a satisfactory bond. The experiment gave a negative result. Considerable pressure was required and even then a bond was obtained only at a few points so that the joint was weak. Also, even with a barely visible gallium coat, the setting time took many hours. The conclusion is that a mixture as described in the reference must be used to obtain a satisfactory bond. Work is under way to try this experimentally early in the next quarter.

D. CIRCUITS

In this quarter, work was done on single-stage logic gates at speeds approaching the Task III goals. No single-stage circuit has been found that meets the test of a worst-case tolerance analysis and there is little hope of discovering one in the time available. As the speed requirements make multi-stage gates unsatisfactory, one of several compromises must be made.

Tightening the tolerances on the components and power supplies might offer a solution if they were not already too tight with multi-stage circuits.

A large number of circuits could be built and then exhaustively tested, with circuits that fail to operate being discarded.

Finally, it is possible to use circuits that may, in some manner, be adjusted individually to insure proper operation. It is this last approach that offers the greatest hope of success.

One quite reasonable method of adjusting a circuit to insure operation is to trim individual resistors after the circuit has been assembled, perhaps by sandblasting, scraping, or grinding. Trimming the components requires the use of wide bandwidth resistors that permit adjustment while remaining stable.

Another way is to use some kind of transistor bias-control circuit for each gate. At once some objections become apparent:

(1) Transistors are big, making the gate physically large, causing signal propagation difficulties.

(2) Transistors dissipate power, making the gate hot.

The objections are best answered by referring to Figure 5-1. The transistors do not make the logic gate large or hot because they are located externally. The transmission lines are terminated for all frequencies by the power supplies, and therefore present a constant resistance to the logic gate. The basic logic circuit is the well known non-linearly loaded monostable circuit. The current source has an output impedance of $R + Z_o$, and part of the power is dissipated in the external power supply. The internal power dissipation in the current-source forming resistor is reduced by about 15 to 20% when compared to a low-impedance power distribution system. The voltage source required is formed by a 1-ohm resistor. Typically, a 100 mv voltage is required, which implies a power dissipation of only 10 mw in the 1-ohm resistor.

One advantage of the coaxial power distribution system is that it eliminates the difficulties and uncertainties associated with the use of a low-impedance, wideband, power-bus system.

A few gates have been built to operate on the external adjustment principle. It was found to be possible to assemble the components of an AND gate or an OR gate in a minimum path-length (less than one inch) configuration inside of a .2 inch x .5 inch x .5 inch metal chassis. The logic connections are made through one .2 inch x .5 inch face and the power supply cables brought out through the opposite face. Gates have been made to work at repetition rates greater than 750 mc with stage delays less than 0.5 nsec with tunnel diodes having peak current-to-capacitance ratios of five to one. It is extremely difficult to gain much information about the operation of the circuits experimentally, as an adequate sampling oscilloscope is not yet available. It is felt, however, that at the speeds of interest the case inductance of the tunnel diodes used is as serious a limitation on speed as the diode capacitance.

A circuit that was investigated this quarter is the basic non-linearly loaded monostable configuration with a GaAs tunnel diode replacing the Ge tunnel diode. There are several ways in which the use of a GaAs unit may improve the performance of the circuit. The most prominent improvement stems from the fact that the diode inductance is primarily determined by the geometry of the diode package, and should therefore be about the same for both kinds of diode. For a given diode peak current, a circuit with a GaAs tunnel diode operates at twice the impedance level of a circuit with a Ge tunnel diode. Consequently, the effect of the diode inductance on the speed of the circuit (the L/R time constant) is half as bad with the GaAs diode.

Another way in which the use of a GaAs tunnel diode improves the operation of the circuit is seen by observing that the non-linearity of the Ge clamp diode is more pronounced when compared to a GaAs tunnel diode than when compared to a Ge tunnel diode. The beneficial effect of a non-linear load line on the recovery time of the circuit should therefore be greatest when a GaAs tunnel diode is used. One minor point that is still worth mentioning is that higher peak-to-valley current ratios are possible with GaAs tunnel diodes than with Ge tunnel diodes.

A check was made on whether or not the use of a GaAs tunnel diode does yield the expected improvement. Two similar logic gates were built, one with a Ge tunnel diode and the other with a GaAs diode with the same peak current and capacitance.

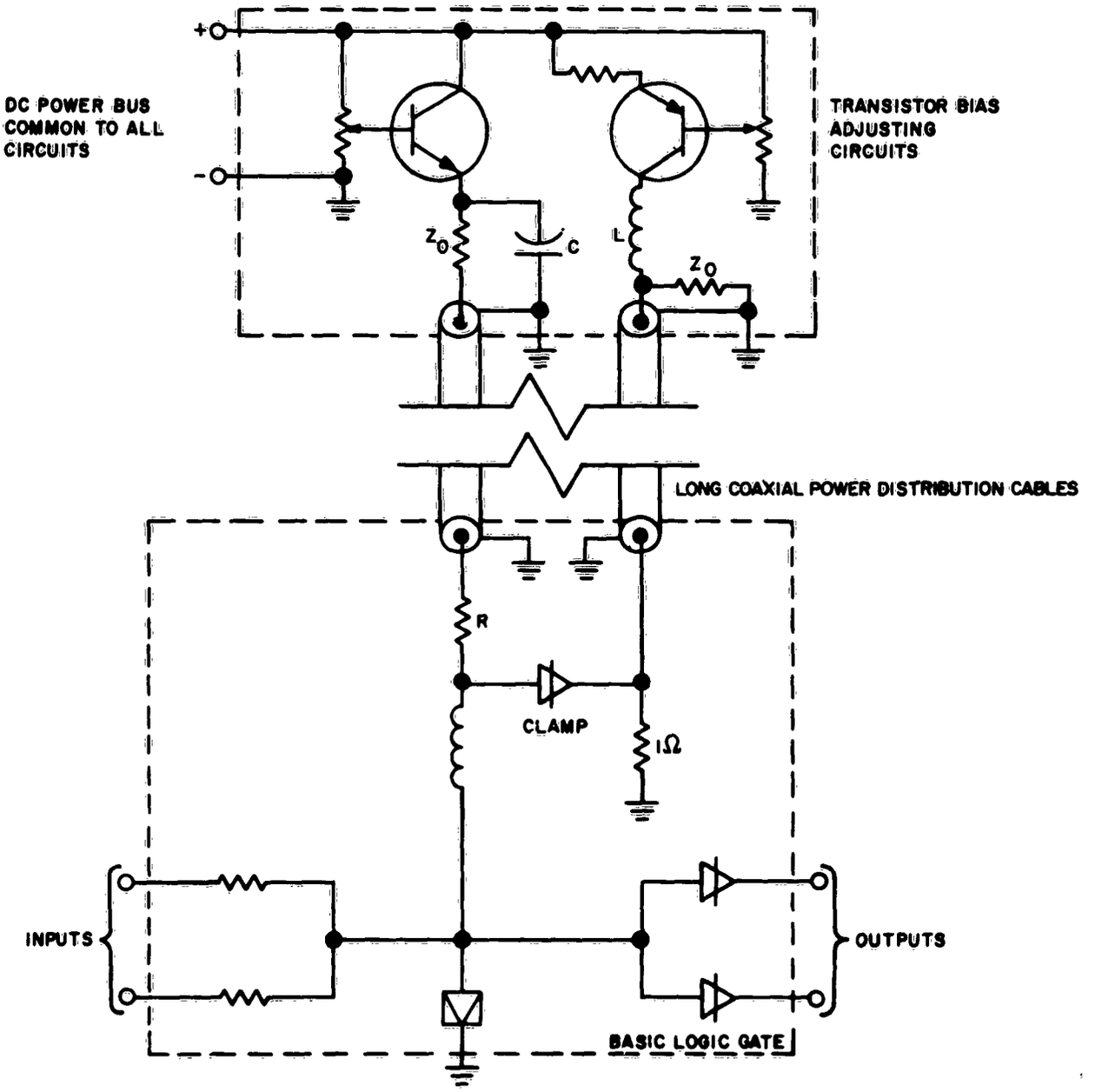

Figure 5-1. Monostable Logic Gate with External Transistor Biasing (1)

The same construction techniques were employed in each case, and the loading was chosen to take equal current from each diode. The circuit with the GaAs diode operated at about a 50% higher repetition rate than the Ge diode circuit. Circuits with GaAs tunnel diodes have been operated at repetition rates greater than 700 mc.

A serious barrier to the use of GaAs tunnel diodes in the high-speed subsystem is the degradation problem. The empirical results described elsewhere in this report indicate that degradation does not occur if the d-c forward current in ma is kept less than .9 times the diode capacitance in picofarads. It is possible that the maximum forward current flow in a diode used in a monostable circuit may be kept below the critical value by heavy static loading or by the use of a small precisely controlled inductor to cause switching to the valley rather than the high state of the tunnel diode. Further work on the use of GaAs diodes is being done.

A single-stage bistable circuit that is under investigation is shown in Figure 5-2. Depending upon the bias conditions and the peak voltages of the diodes, the circuit may be made to operate as a set-reset or as a set-trigger circuit. A positive input to the reset terminal when both diodes are in the high state will force D_2 to switch to the low state. When D_2 is reset it causes D_1 to reset, leaving the bistable circuit in its low state.

The loading effect of L_1, D_3 and R_1 assures that D_1 and D_2 are biased in the valley when the circuit is in its set state. The circuit goes to its set state when an input is applied to the set input terminal. Under some bias conditions, a reset input will cause sufficient current flow through D_2 and D_1 to make the circuit assume the high state if it had been in the low state. This is the set-trigger mode of operation. The bias can be selected, however, to prevent reset inputs from setting the circuit, insuring set-reset operation. Further investigation of this circuit is being made.

E. COMPONENTS

In addition to the tunneling devices being fabricated for Task III and described elsewhere in this report, certain special components have been fabricated; these are described below.

1. Low-Dissipation, Non-Linear Load

The conventional fast-recovery monostable tunnel diode logic gate employs a tunnel rectifier as a non-linear load to enhance recovery time and to provide a current threshold when the tunnel diode is in the low state. To properly position the tunnel rectifier characteristic on the tunnel diode V-I characteristic, it is necessary to employ both voltage and current bias. The current bias required is on the order of the tunnel diode peak current and is generally obtained by placing an appropriate resistor in series with a voltage source of approximately 6 volts. The resulting power dissipation in the resistor is then on the order of 100-500 mw.

This dissipation can be largely eliminated by replacing the tunnel rectifier and current source by a tunnel diode paralleled with a resistor equal to the smallest value of the incremental negative resistance of the tunnel diode. The resulting circuit and load line are shown in Figure 5-3. In order that the load circuit be stable, however, it

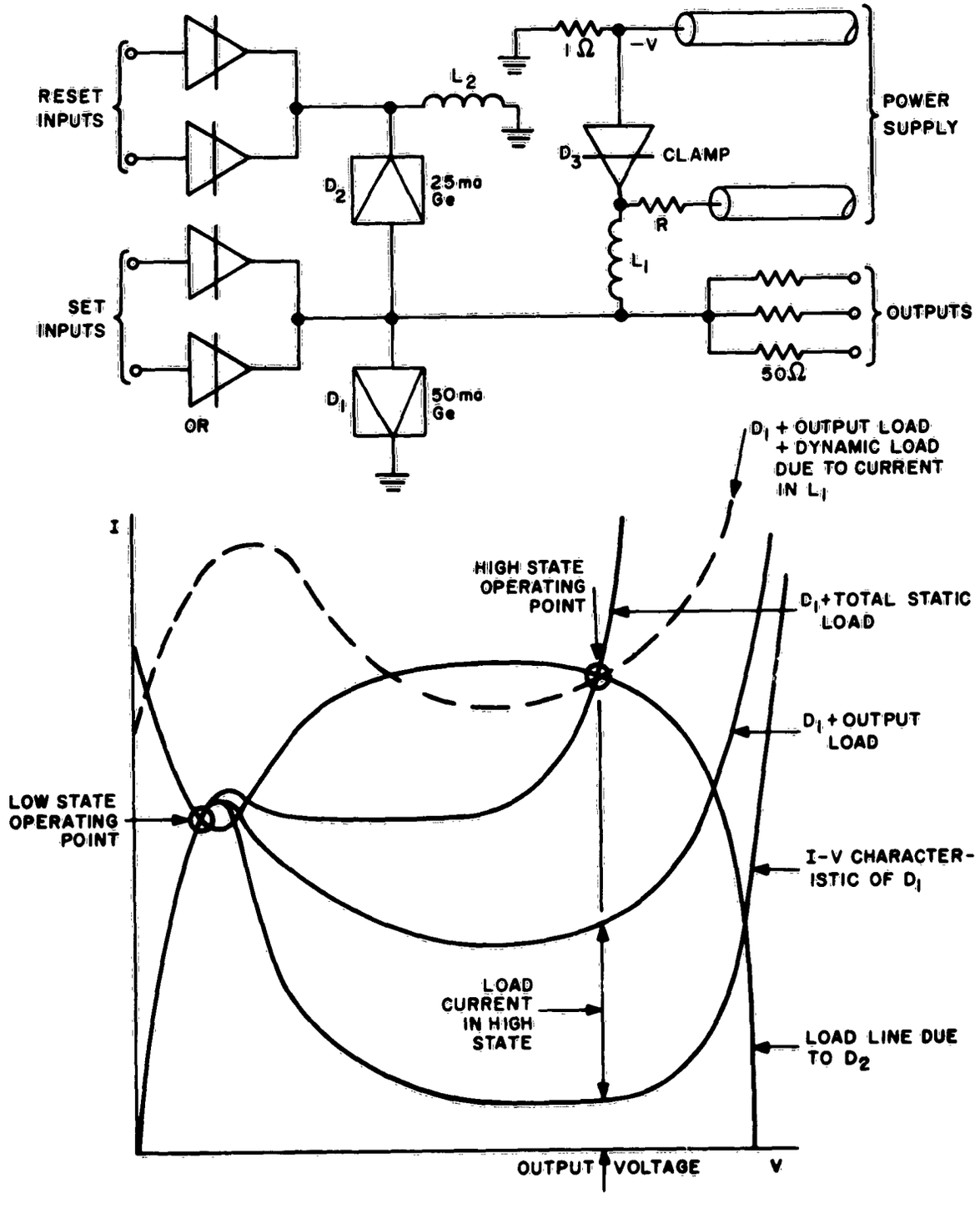

Figure 5-2. Single-Stage Bistable Circuit (a)

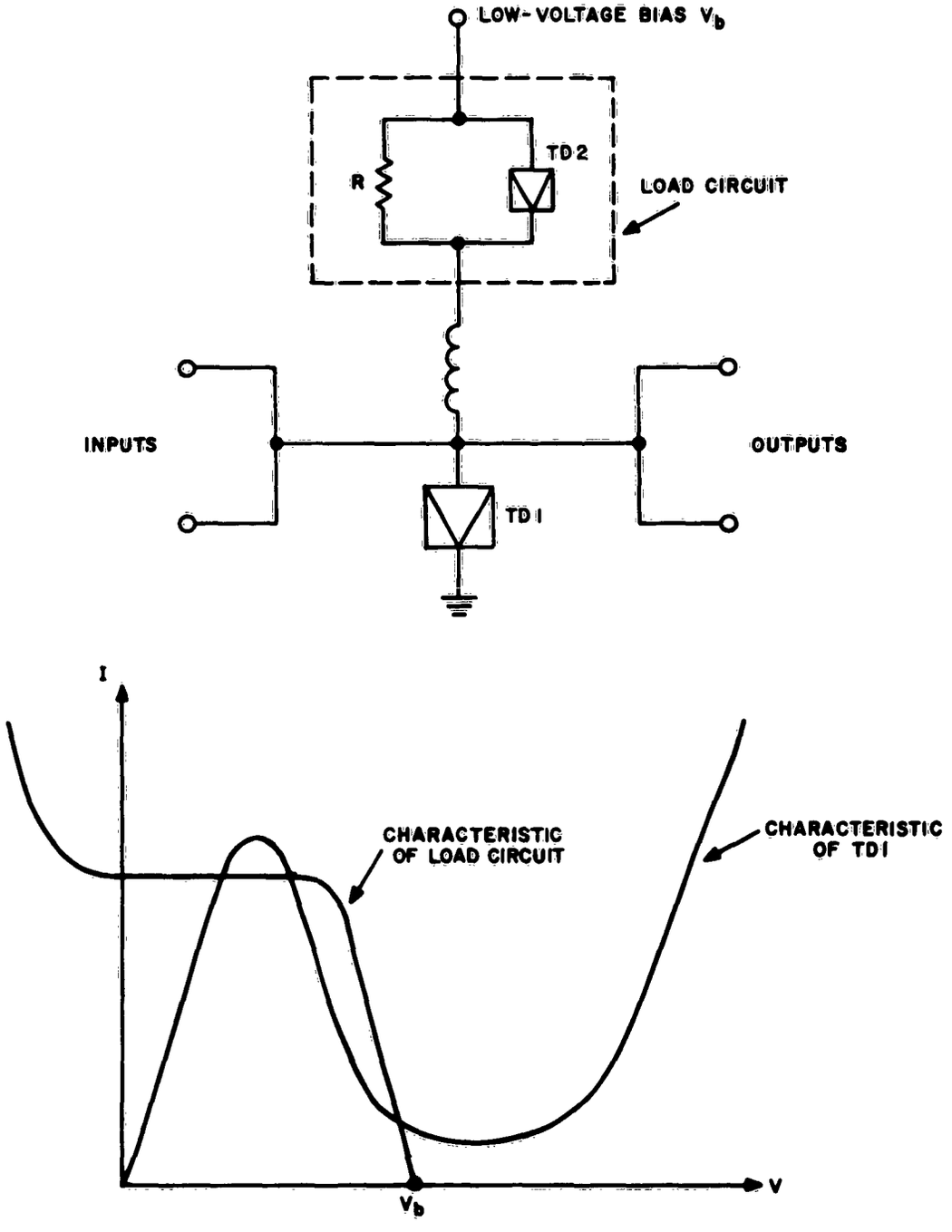

Figure 5-3. Circuit and V-I Characteristic of Monostable Gate with Low-Dissipation, Non-Linear Load (1)

is necessary that the resistor paralleling the tunnel diode have an extremely small series inductance. To accomplish this, a plating method for depositing metal directly across the junction of unencapsulated tunnel diodes has been worked out. The parasitic inductance is thus avoided and stability is achieved. The method works equally well with germanium and gallium-arsenide tunnel diodes and, since the plating process is revisable, precise control of the flatness of the plateau can be achieved. Figure 5-4 shows the V-I characteristics of a germanium tunnel diode at various stages of plating. Control of the plateau current is more difficult since it depends not only on the peak current and peak voltage of the tunnel diode but also on the shape of the negative-resistance portion of the tunnel diode V-I characteristic. Further work is being done to determine whether adequate control of plateau current can be obtained.

2. Inductors

Monostable tunnel diode circuits require an inductor of 2 to 10 nh. In an effort to obtain inductors of these values which are reproducible to close tolerances and which are mechanically interchangeable with tunnel diodes, three units have been fabricated. These units consist of a tunnel diode case with three different configurations of conductors between the end caps. The first unit simply had a fine wire placed axially between the end caps. The others had spirals of wire placed on the ceramic body between the end caps. Preliminary measurements show the first unit to have an inductance of 1.25 nh and the others to have an inductance 2 to 3 times as great.

3. Ferrite Cores

A number of ferrite cores of small dimensions (see Figure 5-5) have been fabricated from a new ferrite material supplied by R. L. Harvey[2]. This material is a cobalt-copper-zinc ferrite with a hexagonal structure fired in a magnetic field. It is expected to have low losses at high switching speeds and may provide a simple means of achieving inversion at speeds close to those required for Task III. Preliminary measurements on these cores, bifilar wound with 5-turn primaries, 5-turn secondaries and connected so as to invert, showed that there is no waveform deterioration of pulses having risetimes of .6 ns. The transformer loss is only 3 to 4 db.

More detailed tests using these cores will be made during the next quarter.

F. MEASUREMENTS

As an aid to close-tolerance tunnel diode circuit development, a measuring bench is being set up with provisions for measuring the equivalent circuit parameters of tunnel diodes and nanohenry-sized chokes, as well as the static peak and valley currents and voltages of tunnel diodes.

Inductance and series resistance of tunnel diodes as well as inductors will be measured by means of a 10-ohm slotted line operated at a frequency near 2 kmc. The line is a well-shielded commercial slotted section modified to accommodate pill-shaped inductors and tunnel diodes, provided they do not have parallel tabs. The low characteristic impedance of the line is of the order of the impedances expected to be measured.

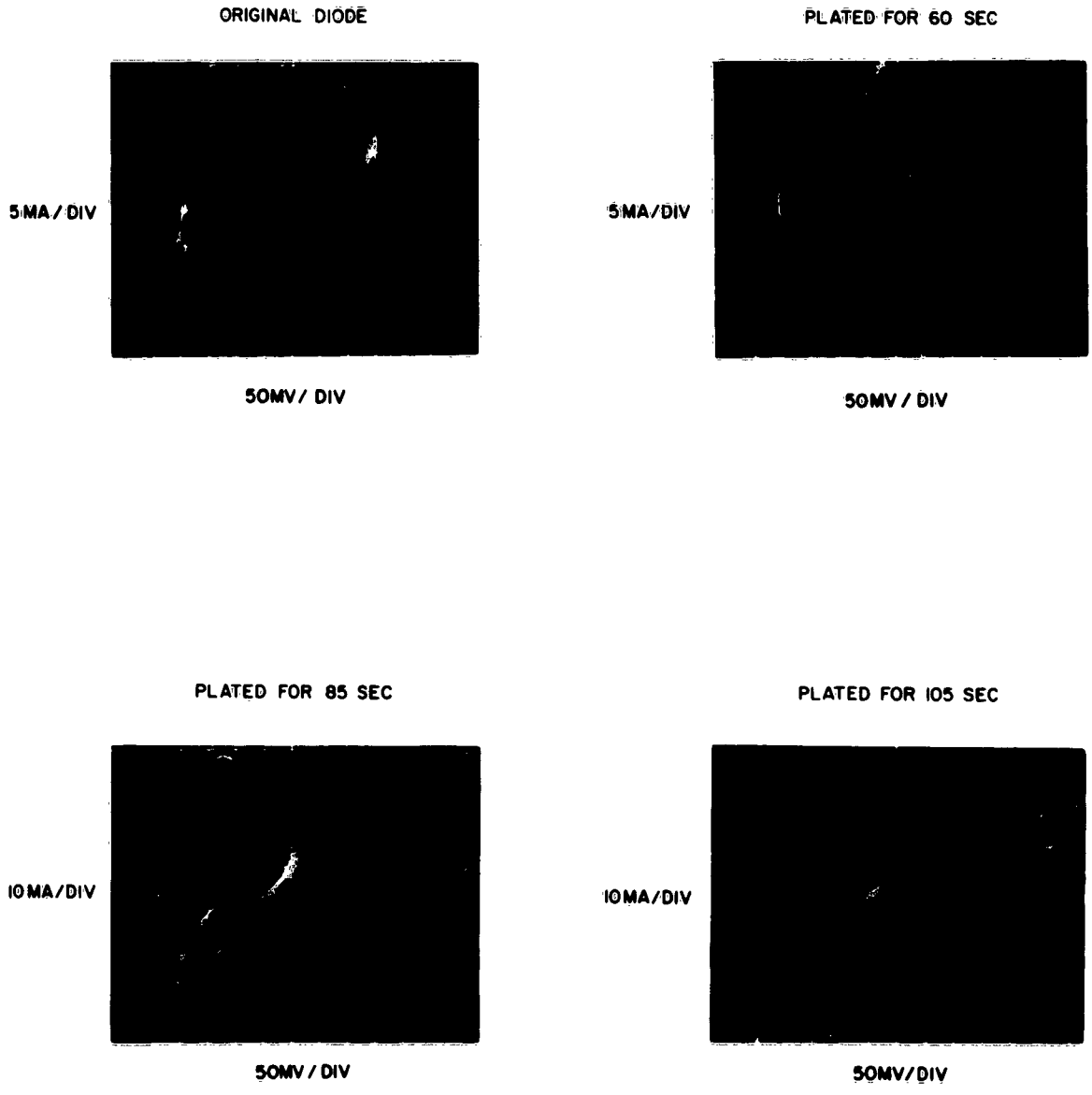

Figure 5-4. V-I Characteristic of a Germanium Tunnel Diode at Various Plating Stages (1)

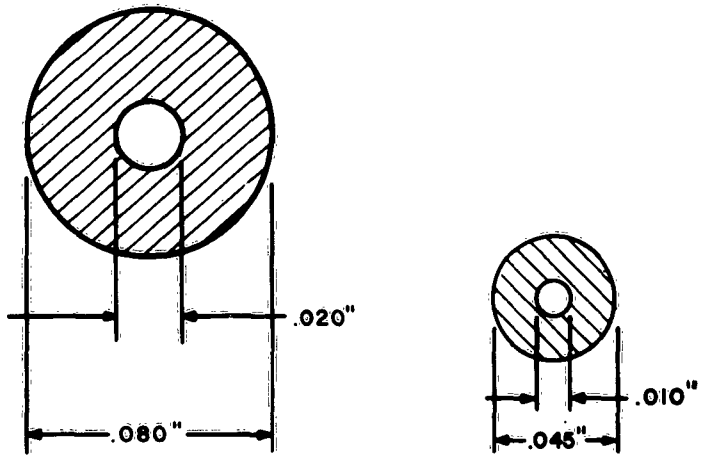

Figure 5-5. Dimensions of Cores Made from Hexagonal Ferrite Material (u)

As soon as it is calibrated and fitted with a biasing current source, this unit will be ready for use. Accuracies of better than 10% are expected.

Peak and valley capacitance will be measured to approximately 3% by means of a Wayne-Kerr type B 801 admittance bridge. This bridge is presently equipped with a mounting jig and biasing source which was designed without regard for stability. A new jig has been designed, and is presently being built, which utilizes a tapped germanium-disk resistor for stabilization during capacitance measurements as well as during static peak and valley current and voltage measurements. Both of these measurements will be made using the same jig and connections.

The static measuring circuit is essentially a duplicate of the one described in the Supplement to Project LIGHTNING Interim Research Report 10-A and has been designed for 0.1% accuracy. This circuit should be ready for use early in the next quarter, shortly after receipt of the operational amplifier which is currently on order.

G. INSTRUMENTATION

1. Ultra-High-Speed Sampling Oscilloscope

The laboratory experimental work on an ultra-high-speed sampling oscilloscope, based on the concept outlined in IRR 10-A, is near completion at the end of this period. Designs of the various stages have been finalized and work is going on at present assembling the various stages into a complete unit. While the feasibility of the system was demonstrated during the last quarter, the practical design, choice and experimental evaluation of circuits and components were carried out during this period. The work involves the following:

a. Countdown

In order to synchronize input frequencies up to 5 kmc, the input tunnel diode monostable multivibrator was designed to have a free-running frequency of about 100 mc.

This was achieved by arranging a disk resistor, made in the laboratory, in the circuit as shown in Figure 5-6. The free-running frequency of the second tunnel diode multivibration is about 10 mc. The circuit diagram of the two-stage countdown used is identical to the one reported before. However, it was found that the bias on the input stage should be adjusted so that it operates as a triggered monostable multivibrator rather than as a synchronized free-running multivibrator.

b. Phase Modulator

The method of phase modulation has been simplified as shown in the circuit of Figure 5-7. Pulses are modulated directly by a low-frequency sine wave voltage. As shown in Figure 5-7, the pulse output of the tunnel diode countdown is applied directly to trigger a bistable multivibrator consisting of two fast transistors. A low-frequency, 60-cycle voltage is applied at the base of one of the two transistors for phase modulation. (This same 60-cycle voltage is also used to sweep the oscilloscope on which the signal waveform is displayed.) The leading edge of the output pulse is thus time modulated by the low-frequency voltage while the amplitude is kept constant. Modulation linearity is found to be within 5%. The output pulse has a repetition rate of 5 mc. This rate is exactly one-half the triggering pulse output rate from the countdown.

c. Pulse Generator

The pulse used to drive the forward biased snap-action diode into backward conduction should have a fast risetime and an amplitude as large as possible, limited only by the peak inverse voltage of the diode. Pulses at 5 mc, generated by the previous described method, fall short of the requirements. Thus, new circuitry is used in the present design. Pulse squaring is achieved by a sharp cut-off pentode (Amperex type 6688) and the subsequent shaping and amplification is done by an ultra-high-frequency tetrode (Amperex type 7377). A negative power supply is used so that the plate may be directly coupled to the load to achieve minimum risetime. The pulse

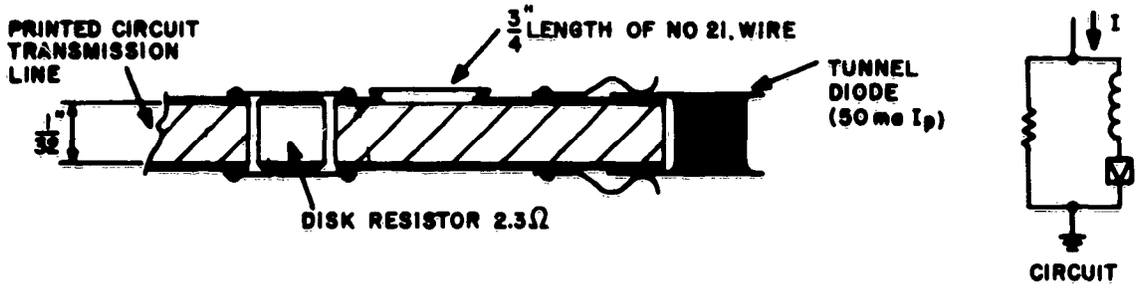

Figure 5-6. 100-mc, Tunnel-Diode, Monostable Multivibrator (u)

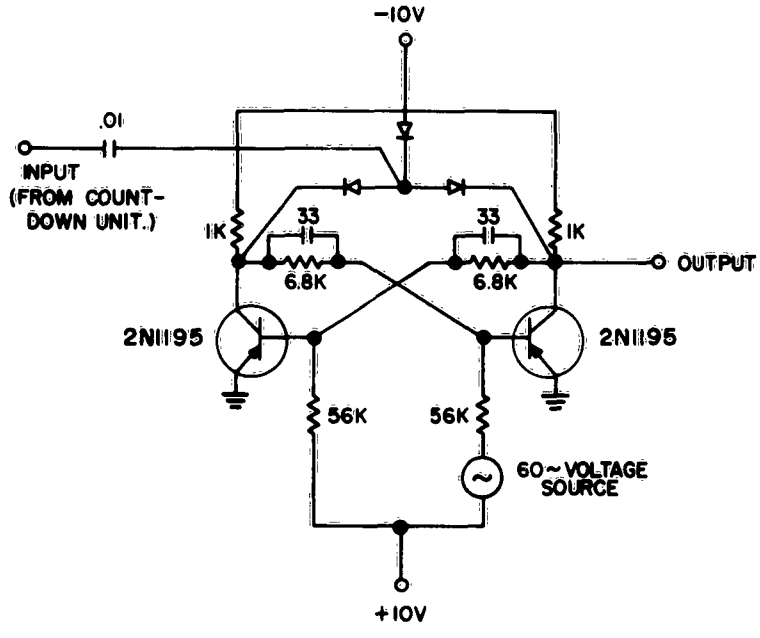

Figure 5-7. Symmetrically Triggered Bistable Multivibrator with Phase Modulation (1)

generator circuit is as shown in Figure 5-8 and the output pulse across a 50-ohm load is shown in Figure 5-9. The risetime, it is believed, can be further improved by using faster switching transistors, such as 2N709's, in the bistable multivibrator. This will be tried early in the next quarter.

III. REFERENCES

1. G. G. Harman: Hard Gallium Alloys for Use as Low Contact Resistance Electrodes and for Bonding Thermocouples into Samples; The Review of Scientific Instruments; Vol. 31, 1960, page 717.

2. R. L. Harvey, I. Gordon, R. A. Braden: Hexagonal Magnetic Compounds; Final Report Contract No. DA-36-039-sc-78288, DA Project No. 3-99-15-108, U. S. Army Signal Research and Development Laboratory, Fort Monmouth, New Jersey.

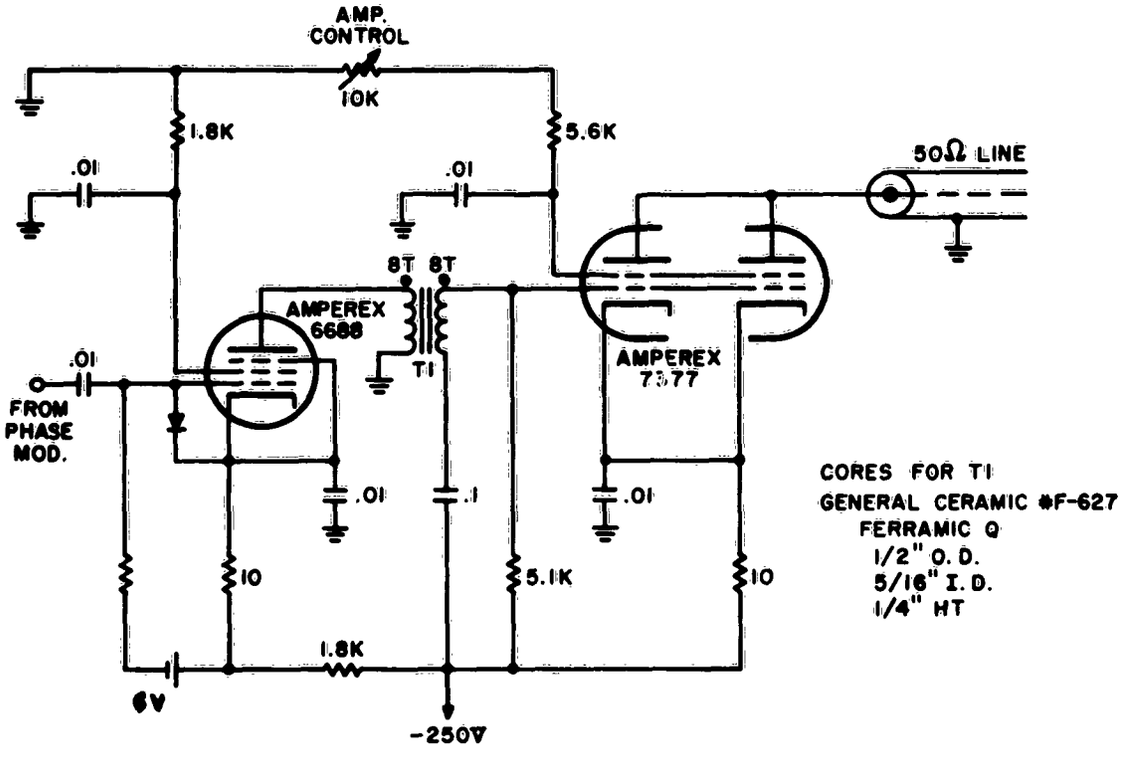

Figure 5-8. Pulse Generator Circuit (1)

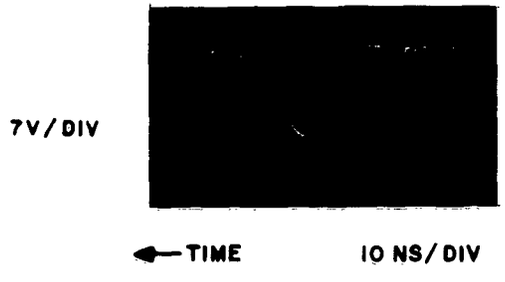

Figure 5-9. Output Waveform Across 50-ohm Load (1)

IV. PROGRAM FOR NEXT INTERVAL

Low temperature solders and gallium-gold alloys will be studied further as potential means of fabricating Task III circuits.

The size and shape of the logic circuit packages for the 40-gate subsystem will be specified and the means of assembly to be used will be chosen.

Monostable and bistable circuits will be investigated further and circuit configurations for the subsystem will be chosen so that component ordering may begin.

Additional low-dissipation, non-linear loads will be fabricated and evaluated.

Additional precision inductors will be built and measured.

The transformers made from hexagonal ferrite will be studied in detail and evaluated for use as pulse inverters.

The tunnel diode high-precision measuring equipment will be completed.

The ultra-high-speed sampling oscilloscope will be completed.

Tunnel diode circuitry for generating clock and control pulses for the 40-gate subsystem will be designed and built.

The logic for the subsystem will be designed.

If sufficient in-tolerance tunneling devices are available, a counter will be constructed and tested using circuits of the type developed this quarter.

Chapter 6. TASK IV – INTEGRATED TUNNEL DIODE MEMORY SUBSYSTEM

SUMMARY

A .030 inch x .030 inch x .060 inch ceramic package for one memory cell is now being developed. The package will contain one tunnel diode, one tunnel rectifier, and one resistor, and will be suitable for use in strip transmission line applications. The problem of individually etching the diode and rectifier in this package has been solved by the use of a protective coating of apiezon wax applied in trichlorethylene solution.

Chapter 6. TASK IV – INTEGRATED TUNNEL DIODE MEMORY SUBSYSTEM

I. PERSONNEL

The following personnel contributed to this phase of the project during the eleventh quarter:

R. D. Gold B. Kashavan H. W. Stetson

II. DISCUSSION

A. GENERAL

The tunnel diode memory subsystem has been described in previous IRR's. A single word contains 32 "bits" or "cells". Each cell consists of a GaAs tunnel rectifier, a germanium tunnel diode, and a resistor, connected as shown in Figure 6-1. During this quarter, work on an integrated memory unit centered about two major problems. The first, how to etch each individual tunnel diode or tunnel rectifier without affecting the electrical characteristics of neighboring units, has been solved satisfactorily. The second, to develop a package suitable for integrated devices in a strip transmission line circuit, also appears to be near a satisfactory solution. In addition, some preliminary work has begun on the fabrication of tunnel diodes and tunnel rectifiers with the required electrical characteristics.

B. INDIVIDUAL ETCHING

At the start of this program it was recognized that individually etching each tunnel junction would be a major problem. This was verified experimentally by alloying two tin dots on a 25-mil GaAs pellet in a single package, and attempting to etch one diode thus formed without changing the characteristics of the other. Etching was performed by immersing the wafer in a 40% KOH solution and passing an etch current of 300 ma for ten second intervals through one diode only. It was found that both junctions etched

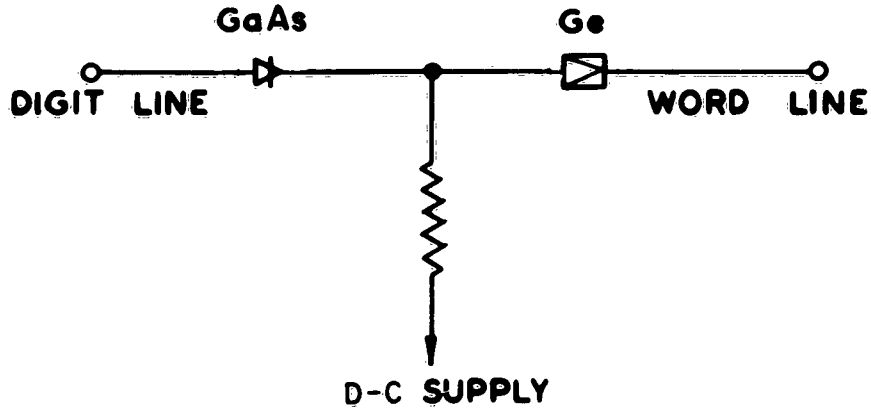

Figure 6-1. Basic Memory Cell Circuit (a)

at about the same rate. To avoid this, it was necessary to mask one diode with a protective coating while the other was being etched. Several techniques for accomplishing this were explored.

A ceramic wafer with a large number of closely spaced holes was prepared, and tunnel diodes were mounted in each compartment. One technique tried was to fill only one compartment at a time with the etch solution, blotting any excess solution with filter paper. The dot was found to etch more rapidly than the p-type GaAs pellet, probably because the small quantity of etch solution in the diode compartment quickly became saturated with dissolved GaAs. Other techniques tried included the use of rubber plugs to prevent the etch solution from coming into contact with diodes not to be etched, and the use of a glass slide with a hole to accomplish the same purpose. Both techniques were only moderately successful. However, it was found that a tunnel diode could be completely protected from the etchant by covering it with a suitable wax. Wax dissolved in trichlorethylene (TCE) was applied to the diode. The TCE evaporated rapidly, leaving the diode completely covered by the wax, which is impervious to the etch solution. This technique should work equally well when diodes are mounted in the package described below.

C. MEMORY CELL PACKAGE

Considerable time has been spent on the development of a package for an integrated memory cell. This package should be suitable for strip transmission line applications and should require no "blind" soldering. Several large-scale models were made in order to anticipate problems which might arise in the fabrication of the actual package, and also to serve as demonstration models. Work has now begun on a ceramic package with outside dimensions of .030 inch x .030 inch x .060 inch. This is a reduction in the total volume per cell by a factor of four, as compared with the originally proposed cell dimensions. This package, shown in Figure 6-2, will contain individual compartments for the tunnel diode and the tunnel rectifier (to facilitate individual etching), and an evaporated film resistor.

The package will be made of high-alumina ceramic using molybdenum-manganese metallizing for conducting paths and semiconductor mounting areas. The ceramic is built up from alumina-loaded sheets of thermoplastic vinyl which are laminated together under heat and pressure and sintered to a dense ceramic. Wherever metallic areas are desired, such patterns are "silk-screened" on the sheets using a molybdenum-manganese paint. If such areas are within the body of the ceramic, then other sheets are laminated over the ones bearing the metal pattern. Holes are punched in the unsintered sheets using ordinary metal-working dies. Sheets having holes are laminated to sheets without holes to form cavities with bottoms. Two such cavities, with appropriate metallizing, will be used as a "unit cell" of the integrated memory subsystem.

At the present time, holes have been punched of approximately the required size with the desired separation between holes. "Firing" has been successful. Based on this early effort, the dimensions of the new package are believed to be within the physical limitations of the technology used. Equipment is now being assembled for the vacuum deposition of thin film metal resistors.

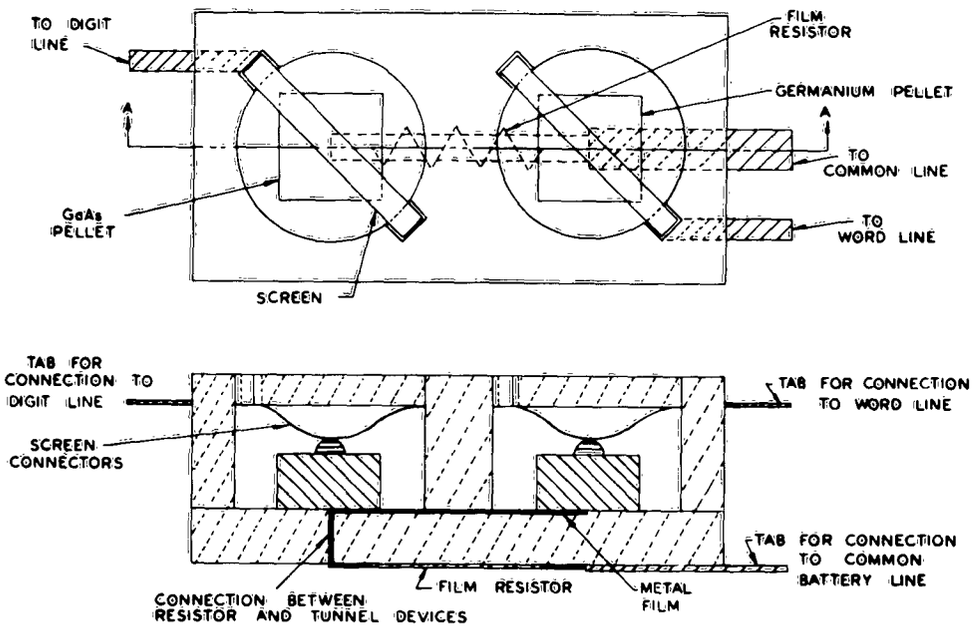

Figure 6-2. Details of Basic Memory Cell (u)

D. TUNNEL DIODE AND TUNNEL RECTIFIER FABRICATION

Some experiments were carried out to form a germanium-gallium arsenide heterojunction. Such a junction permits the fabrication of both the germanium tunnel diode and the gallium-arsenide tunnel rectifier directly on one germanium wafer. The results of these experiments, however, indicated that it would be extremely difficult to make devices to the desired specifications using the heterojunction technique. It was therefore decided to make germanium tunnel diodes and gallium-arsenide tunnel rectifiers individually. Furthermore, the results of the etching experiments described above made it obvious that there would be no advantage in making a single cell with a single crystal.

The dimension of the pellets required for the integrated package is about .010-inch square, instead of the .020-inch or .035-inch size with the two conventional packages.

A few germanium tunnel diodes, using 10-mil pellets and the standard diode package, have been fabricated into devices within the required specifications. In this method, dots containing arsenic are alloyed to highly doped p-type germanium pellets. The alloyed pellets are then mounted in packages and electrolytically etched to the required peak current values.

It is more difficult to make 10-mil pellets of GaAs because it is more brittle than germanium. In view of this, a few experiments have been successfully carried

out to make 10-mil pellets of GaAs. The inert junction technique, described in the previous IRR, is being used to make tunnel rectifiers.

These tunnel devices will be mounted to the integrated device package and will be etched individually to the required specifications.

III. PROGRAM FOR NEXT INTERVAL

A prototype memory cell will be fabricated.